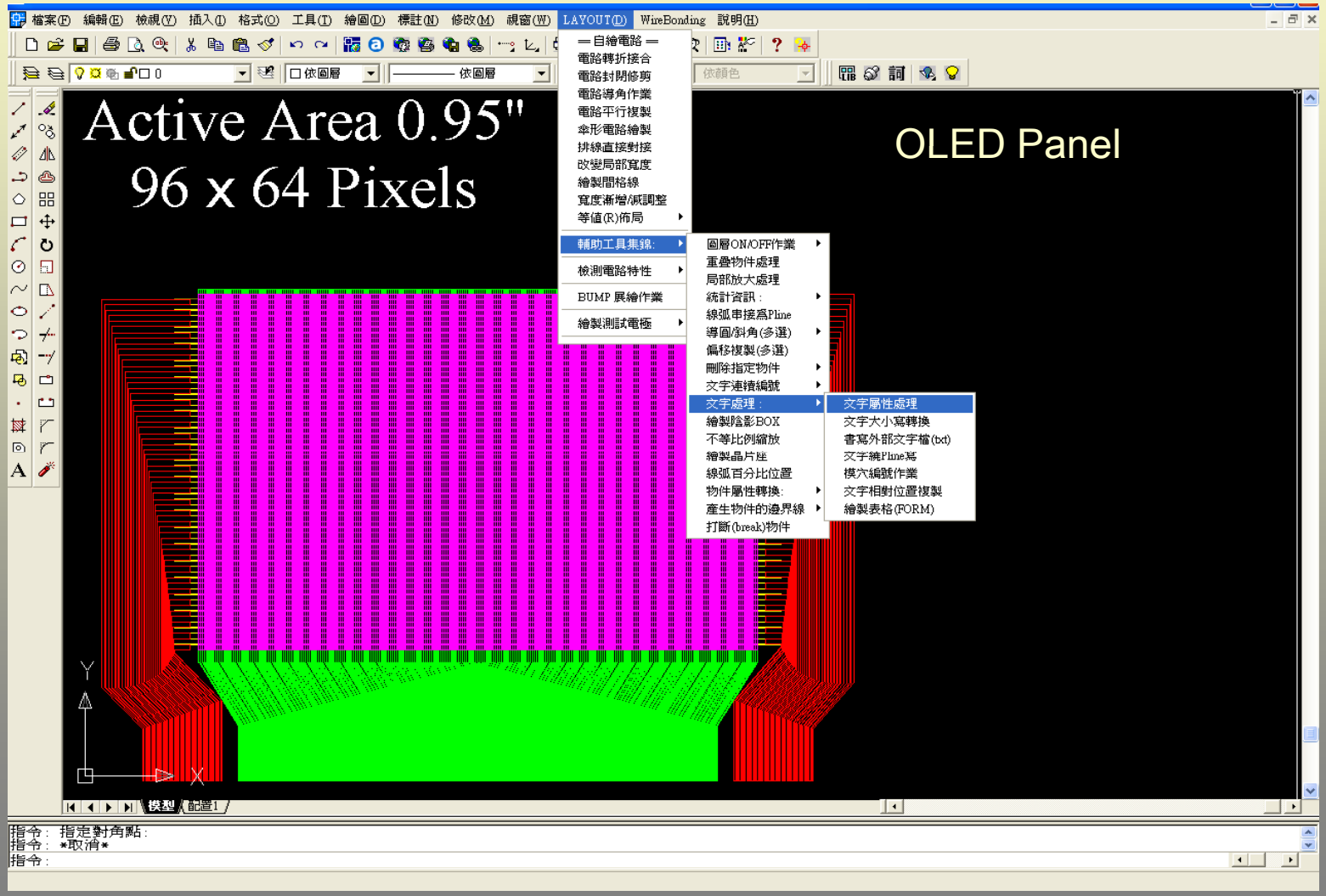
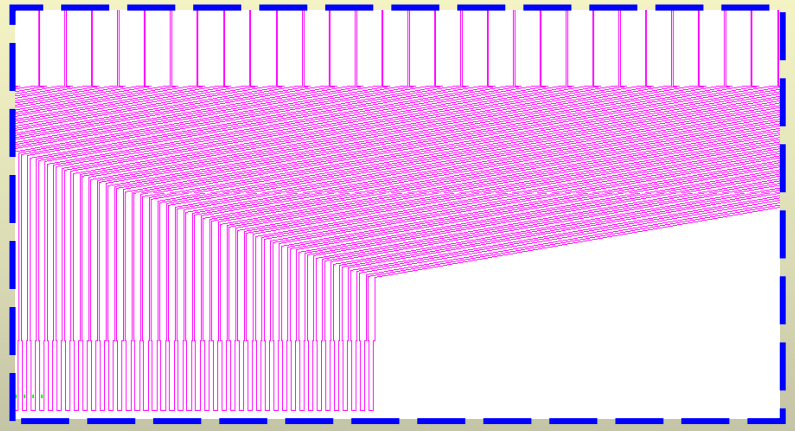
Gtools ITO trace layout&checking tools

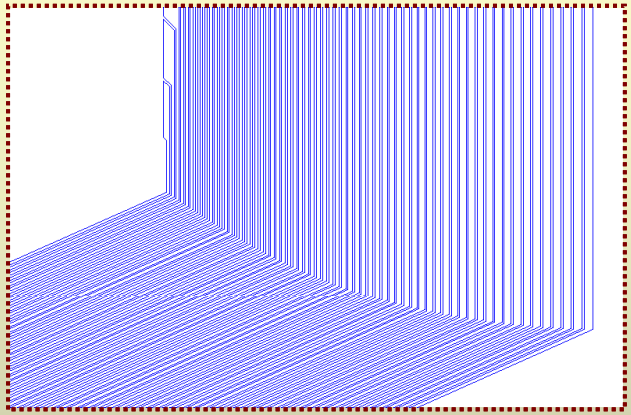
(for AutoCAD based)

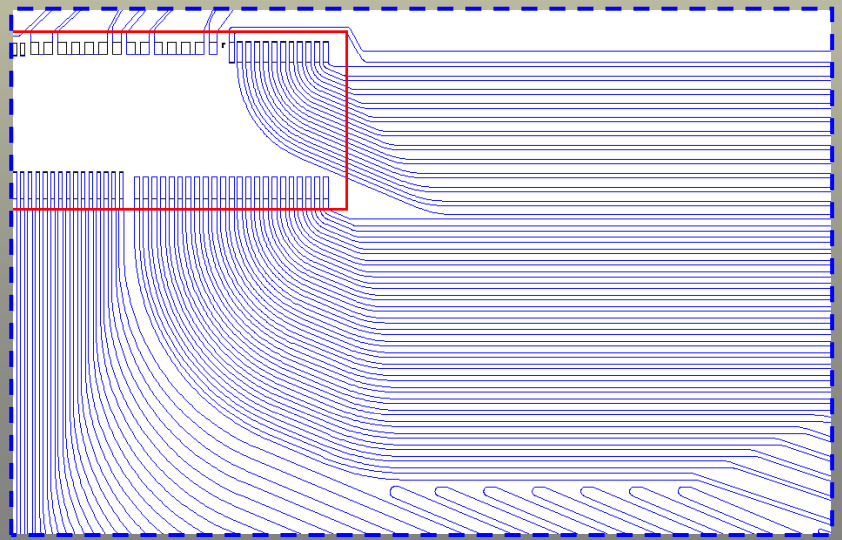
1. Electric circuit support to layout　2. Electric circuit examination and adjustment　3. support to facilities tool collections

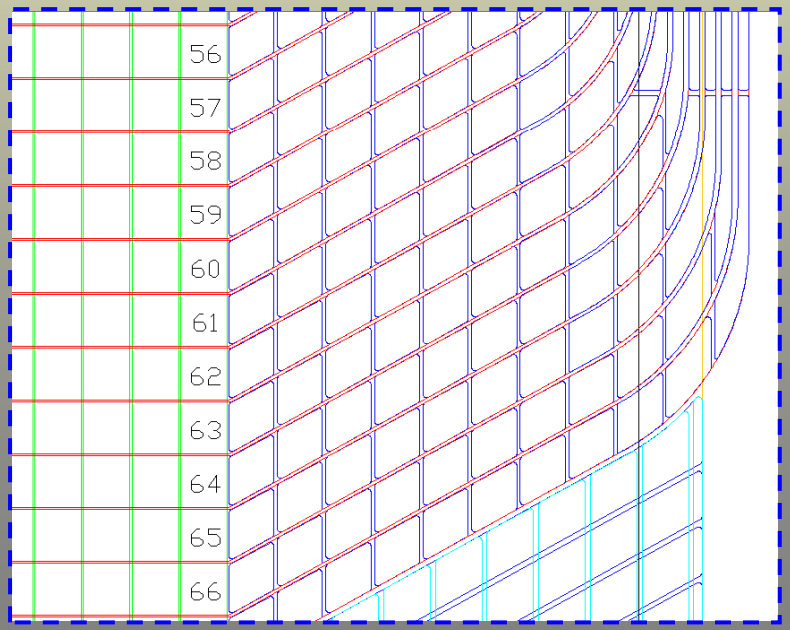


(壹)CSTN/STN LCD/OLED ITO electric circuit support to layout





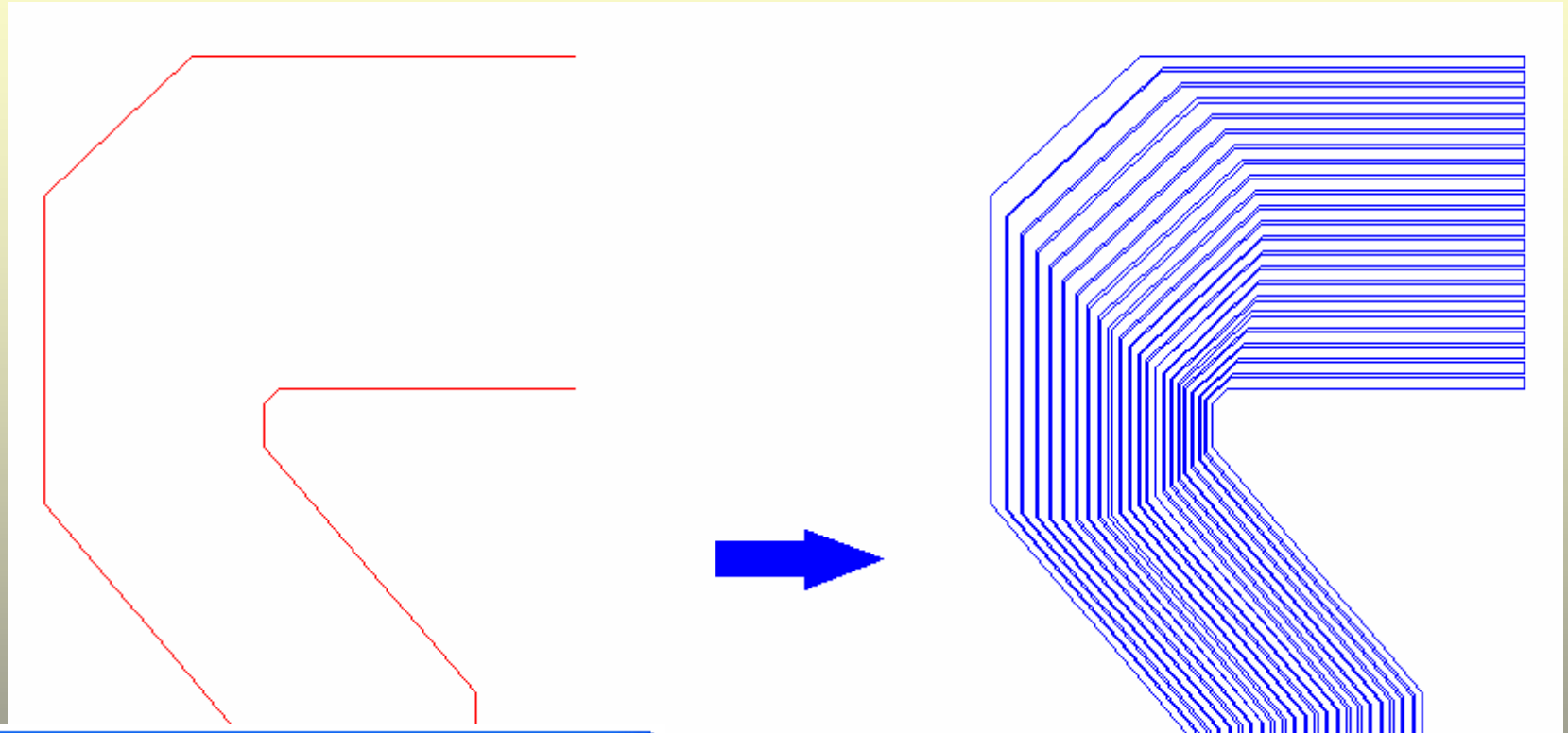




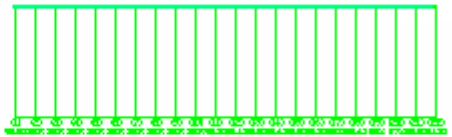
(1).

In the scope equal electric resistance auto layout

Within the scope of limited space, auto layout the optimization R(equal R), can also be worth in the R of appointed each electric circuit inside the excel



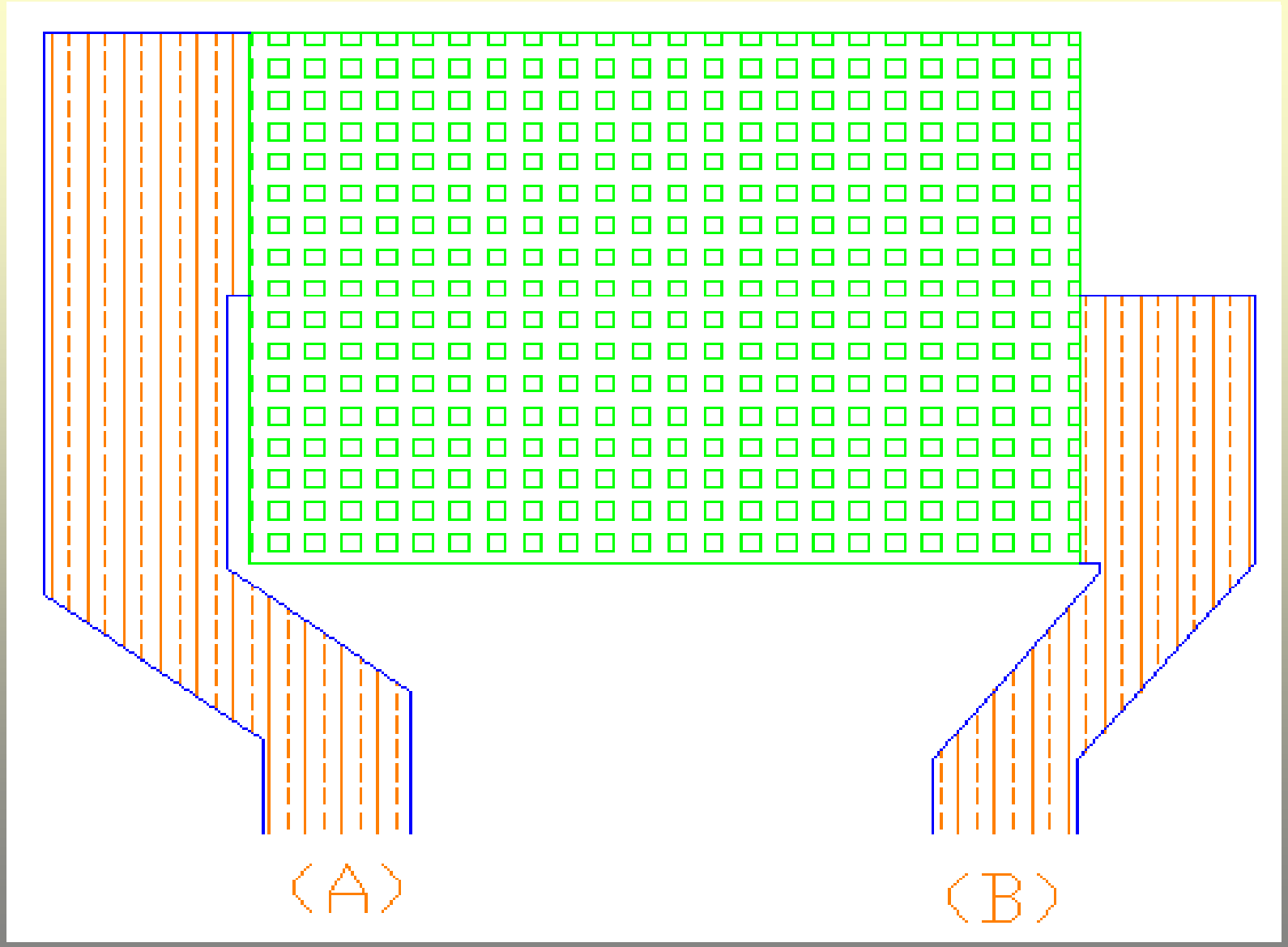
	A	B	C	D	E
1	No.	Optimize	Max R	Min R	Expect R
2	1	76.41685479	257.6604339	71.58325891	80
3	2	76.49078253	266.7916148	73.47533978	80
4	3	76.49078253	274.0953752	74.88740229	90
5	4	76.49078253	281.6875444	75.82067623	90
6	5	76.49078253	289.6642584	76.32624772	95
7	6	76.49078253	298.1216535	76.49078253	95
8	7	76.49078253	307.155866	76.41961945	100
9	8	76.49078253	316.8630321	76.2217803	100
10	9	76.49078253	327.339288	75.99880139	90
11	10	76.50009644	343.0798345	75.83703277	90



(common area autolayout) 阻值曲率圖

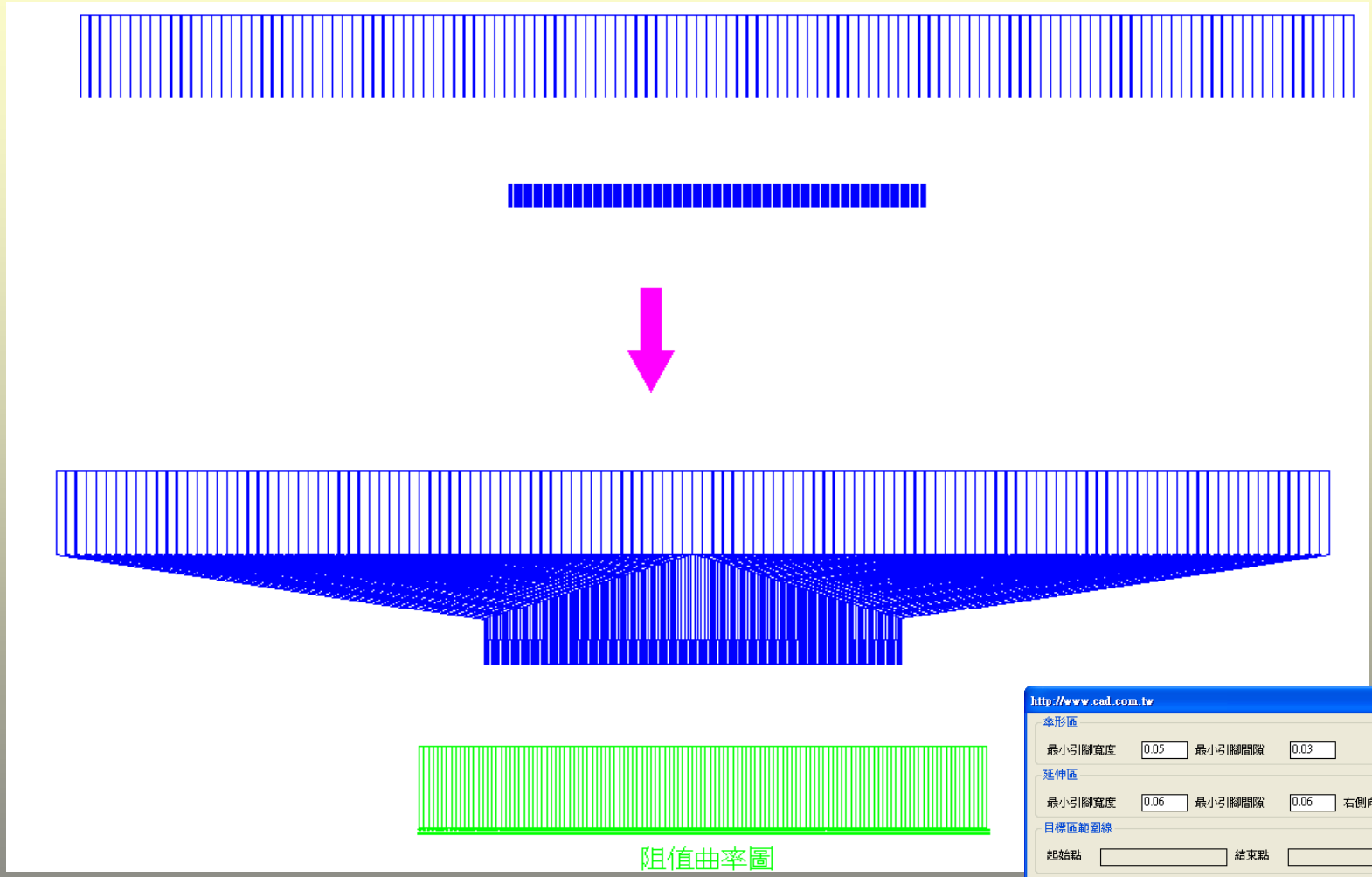
(1-1).

Common trace auto equal-“R” layout (A=B)



(2).

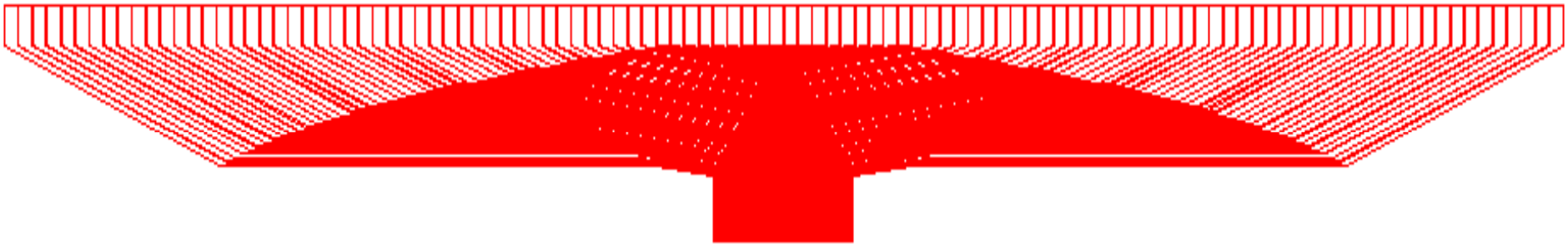
Electric circuit of fan equal R autolayout



(segment area autolayout)

Segment 區直接佈局等R的接合電路

Segment and common multi application

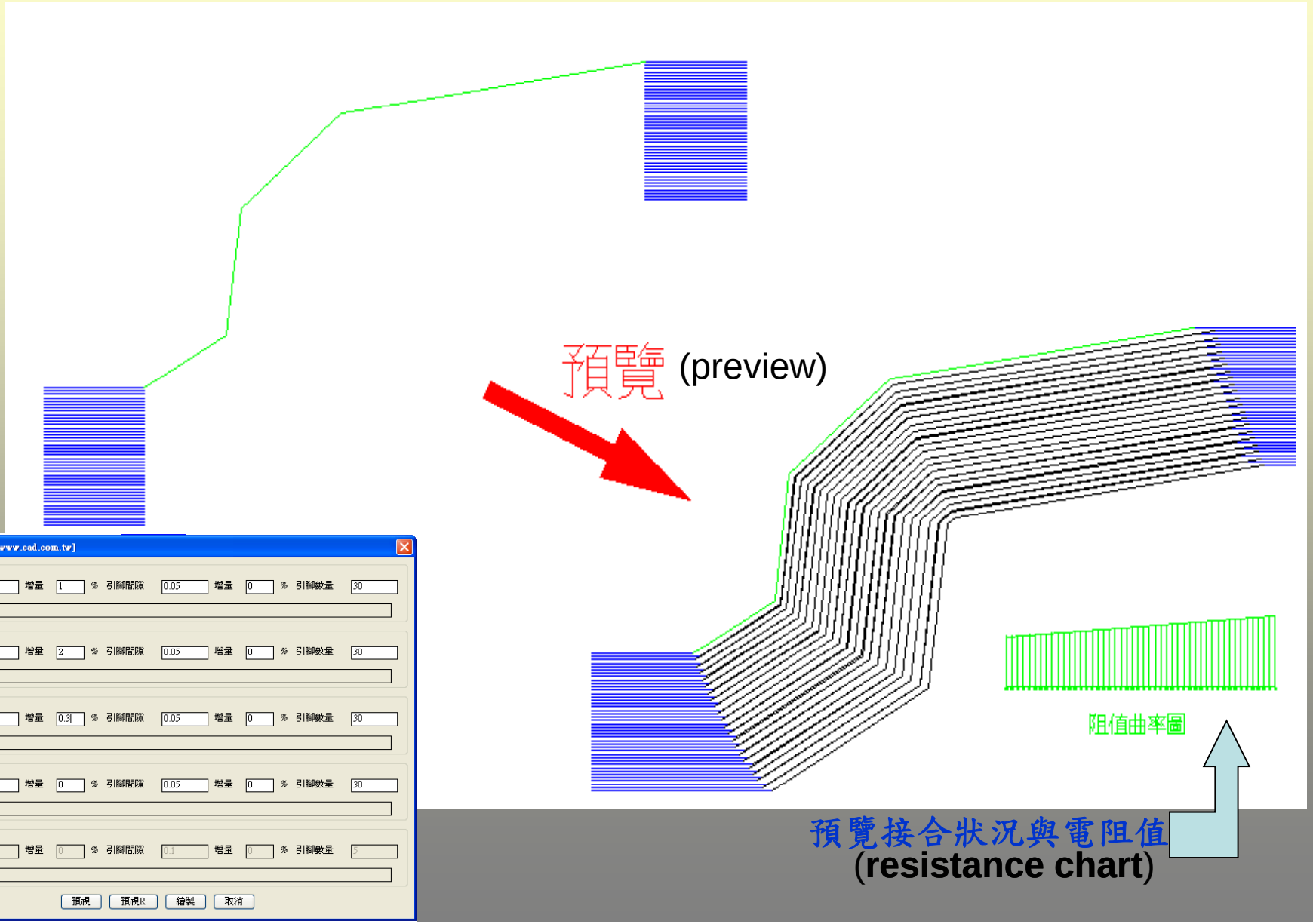


傘型擴充的等R佈局

(3).

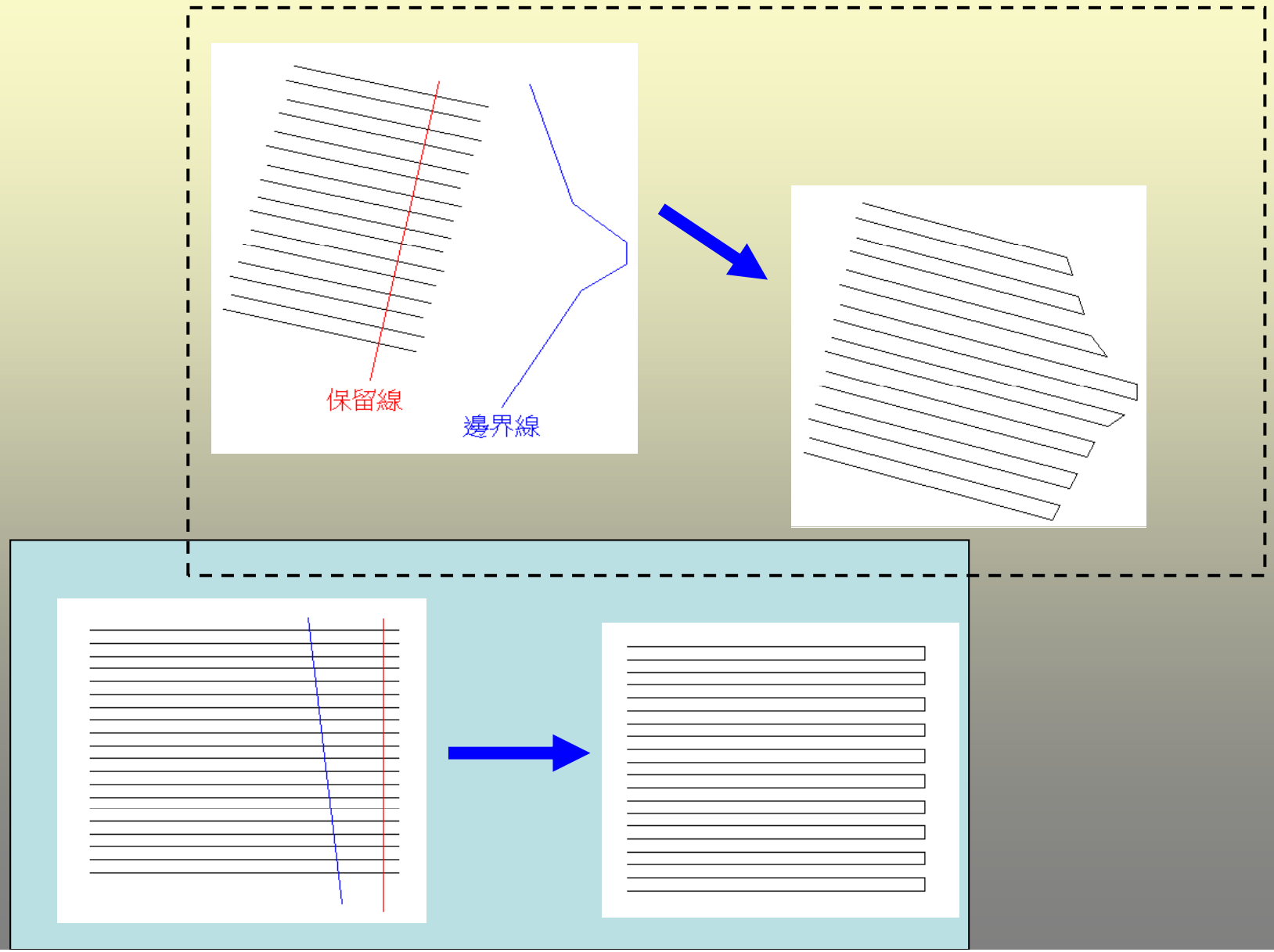
Preview the resistance chart and final layout

可於交談框內即時調整 **width** 以利阻值均化



(4). Trace edge closed by reference line

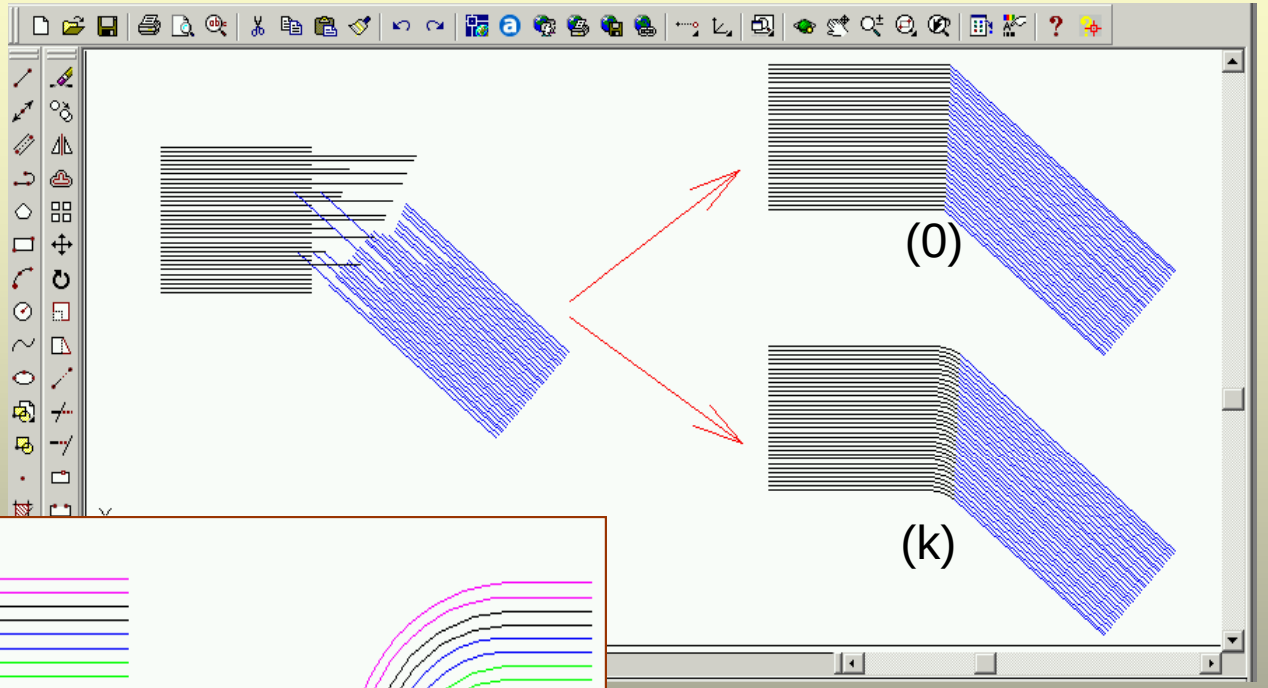
電路快速封閉延伸與修剪

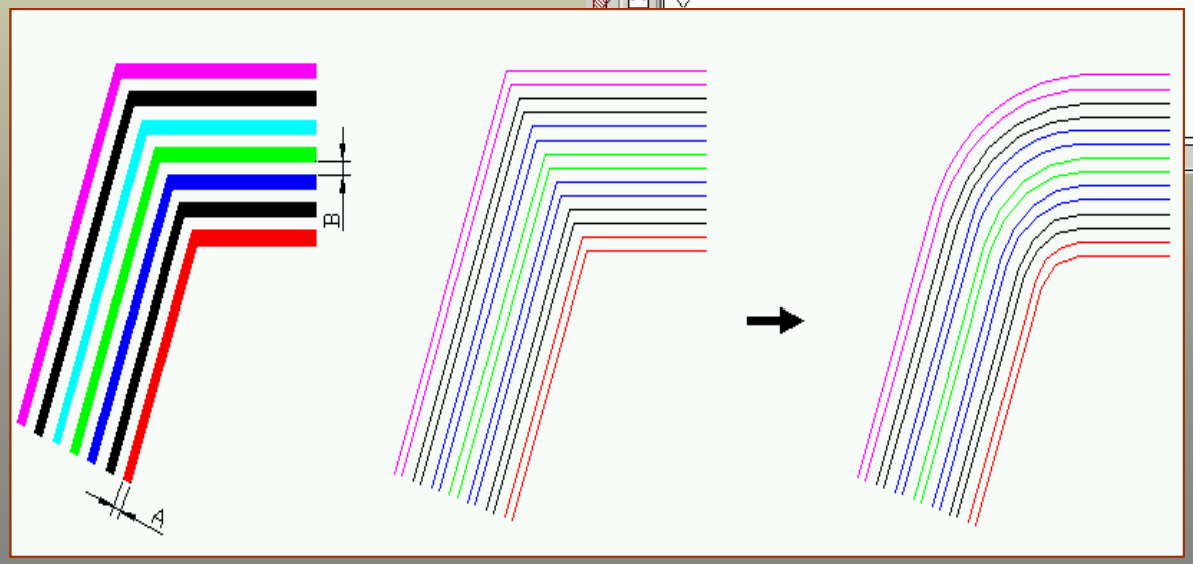


(5). 兩端電路相接與快速導角作業

Auto link and fillet

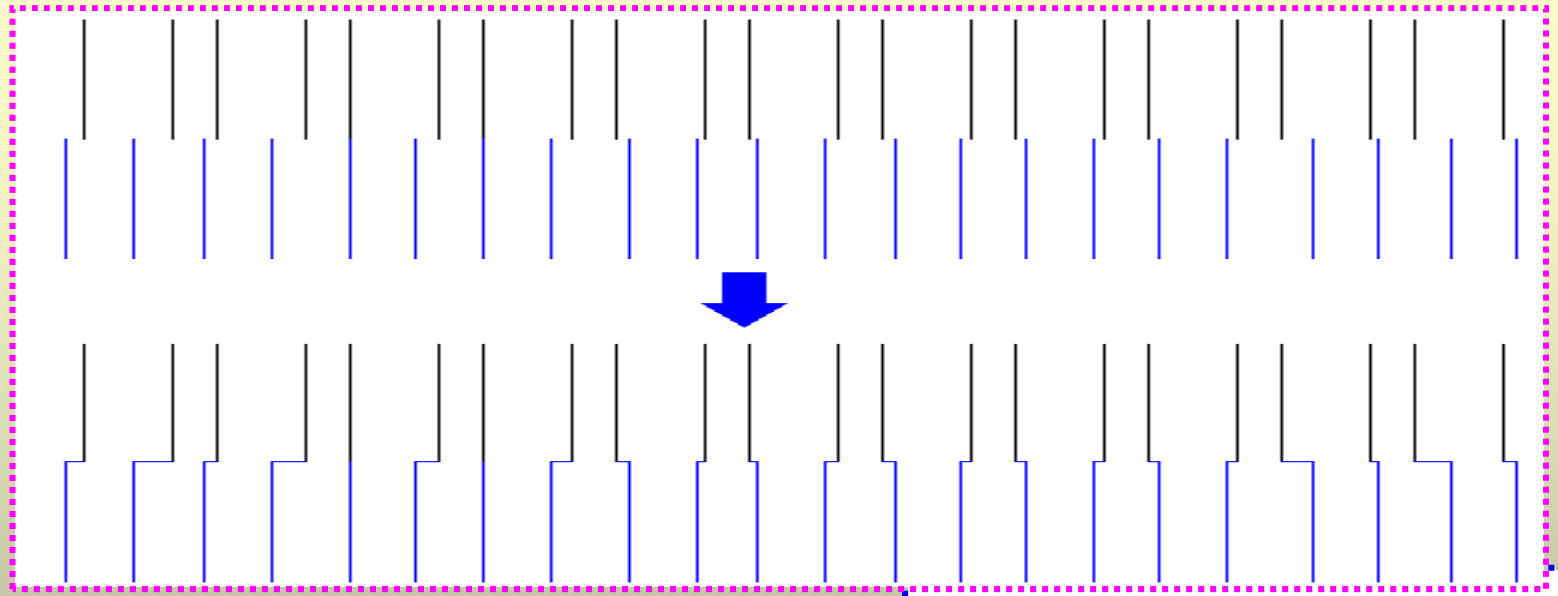
Radius = 0 V.S Radius = K

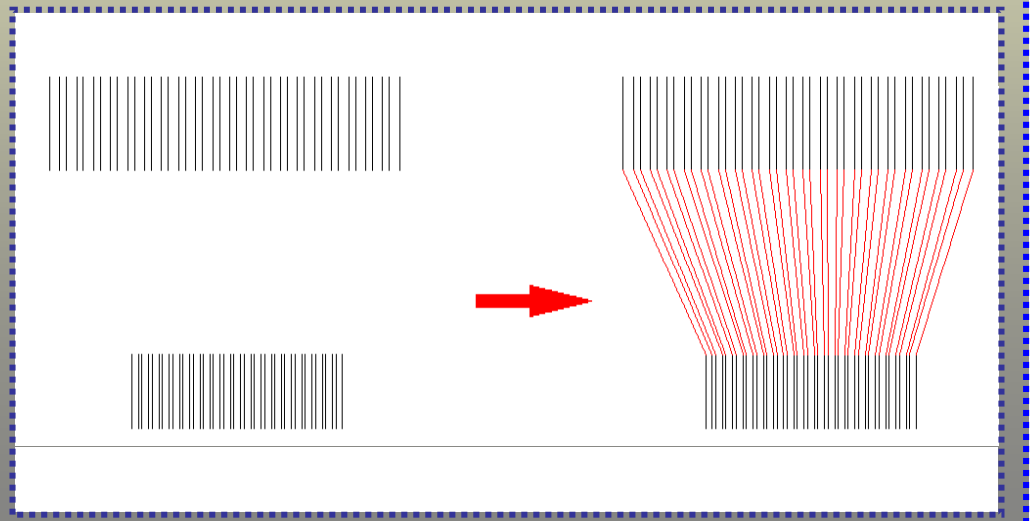


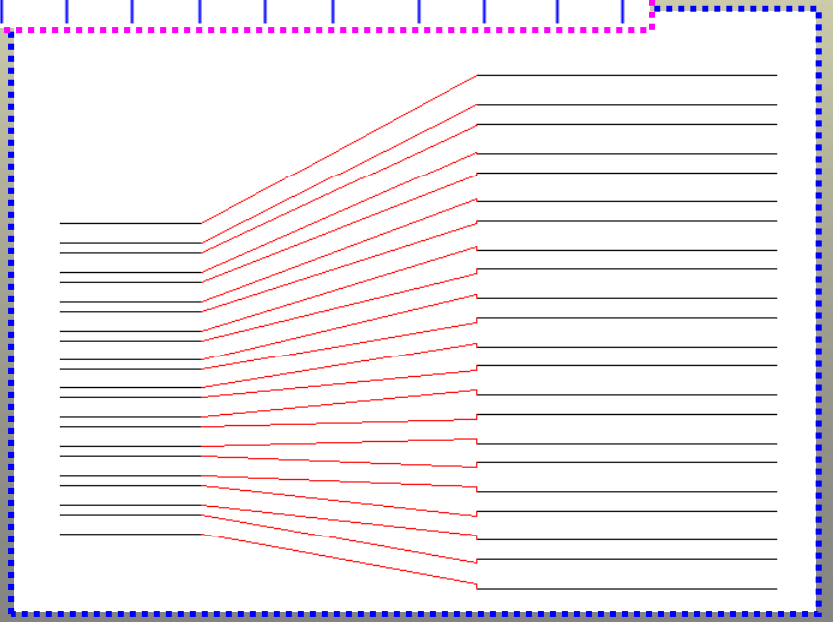


變化 **R** 應用 **(Variety** radius)

(6). **Auto link of Trace end-point**



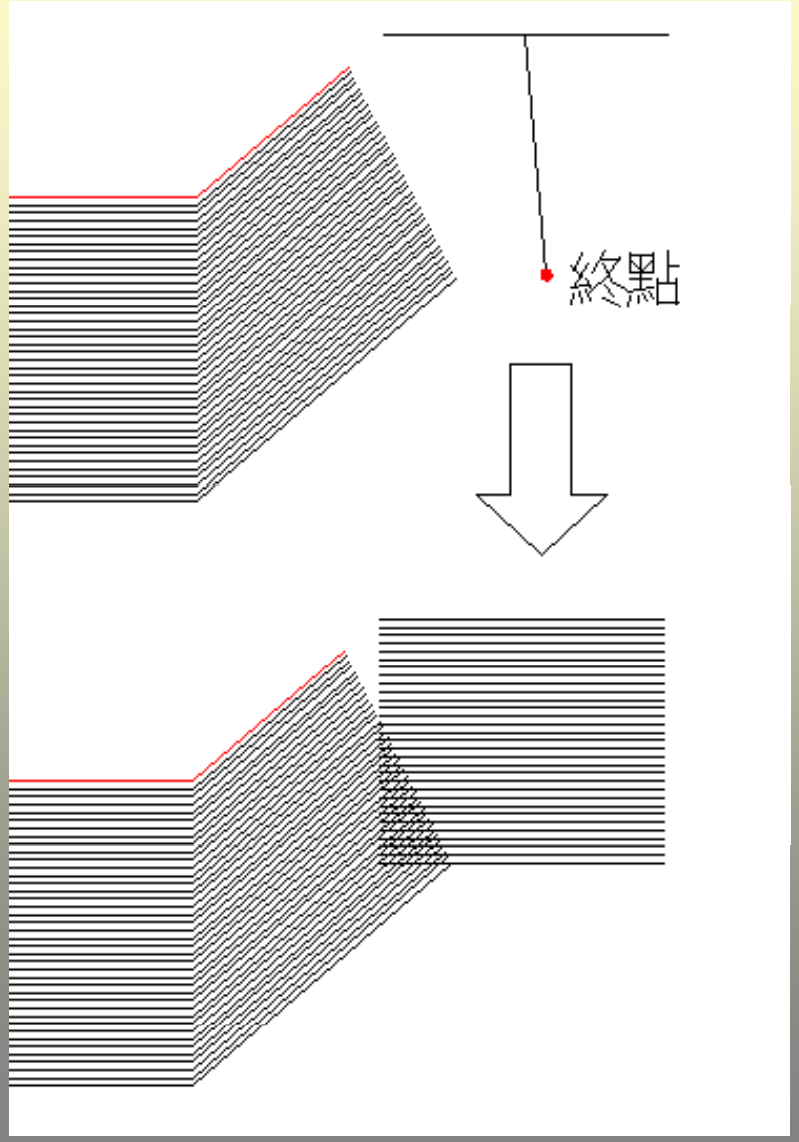


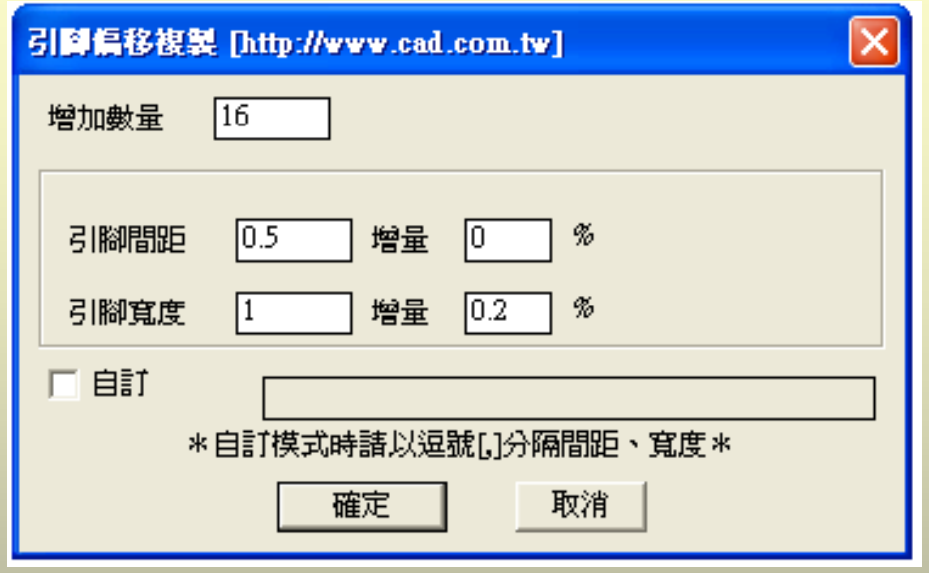


(equal R of link)

(7).

Trace offset and copy





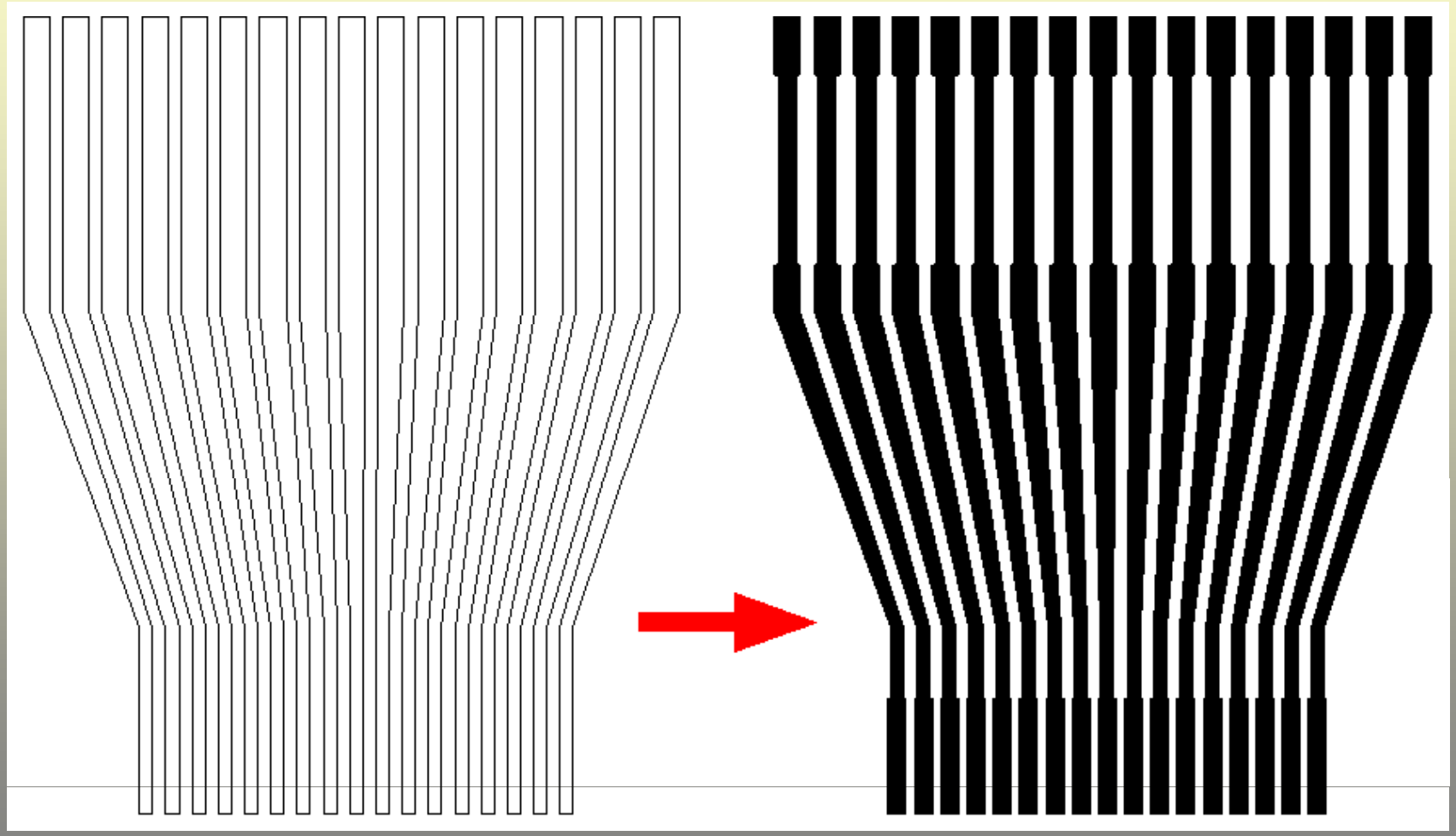
1. 偏移複製不限方向 **(offset to any direction)**

2. **Increase quantity** of **width & space**

(8).

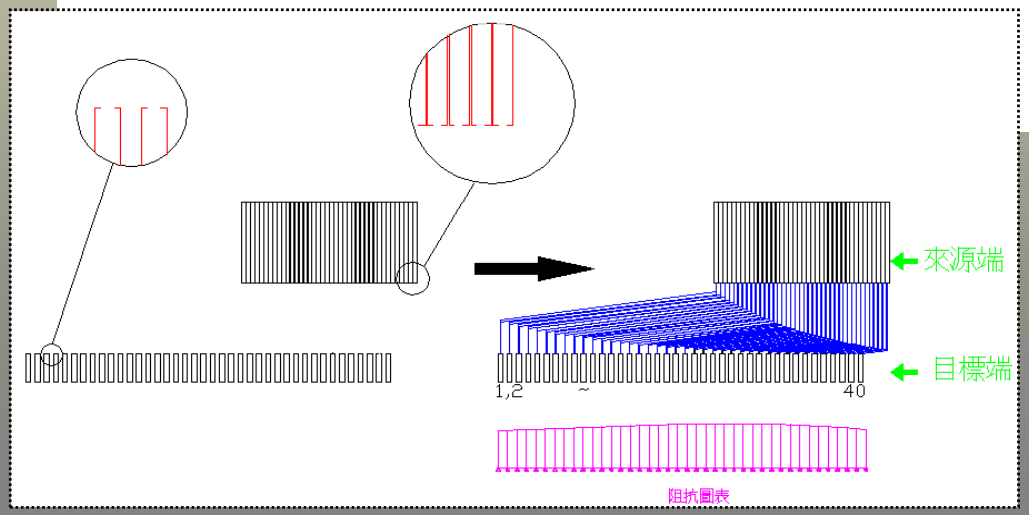
批次改變電路的局部寬度

(Change width of trace part)



(9).

電路延伸轉折連接



自動產生紅色接線

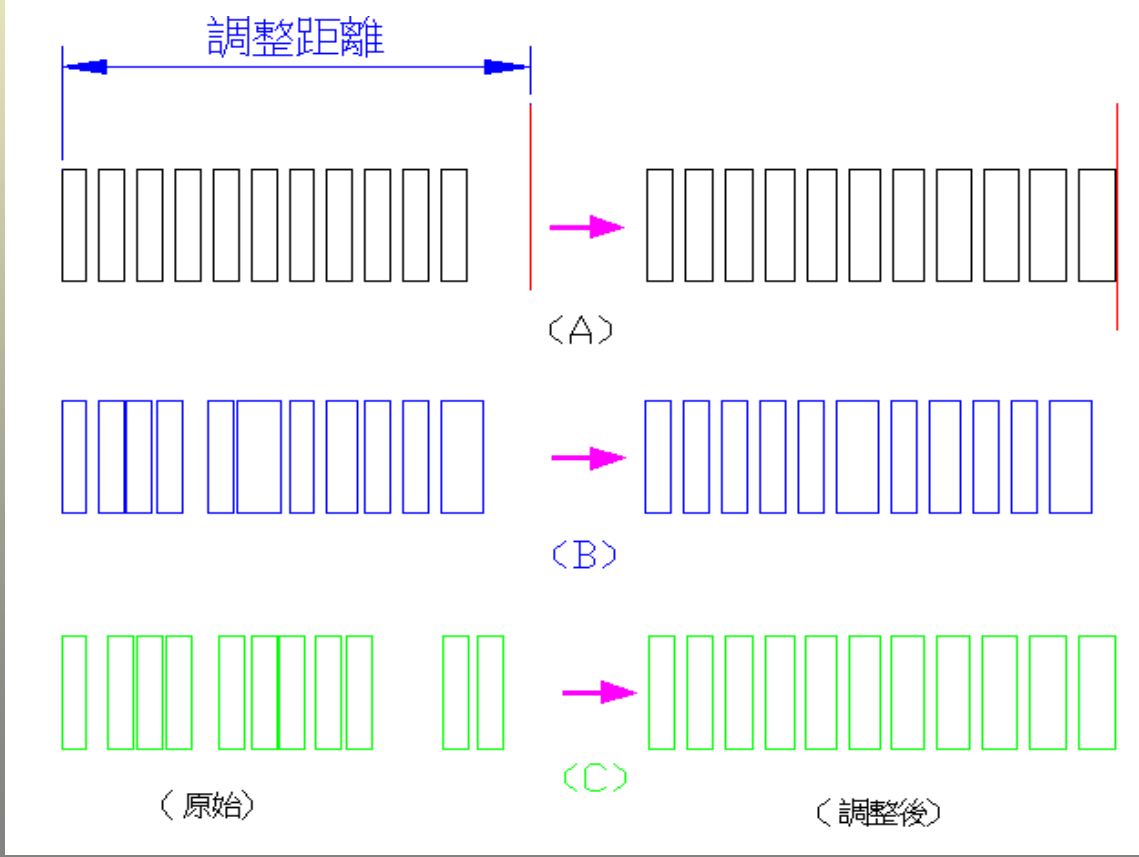
(Generation red line for link)

(10).

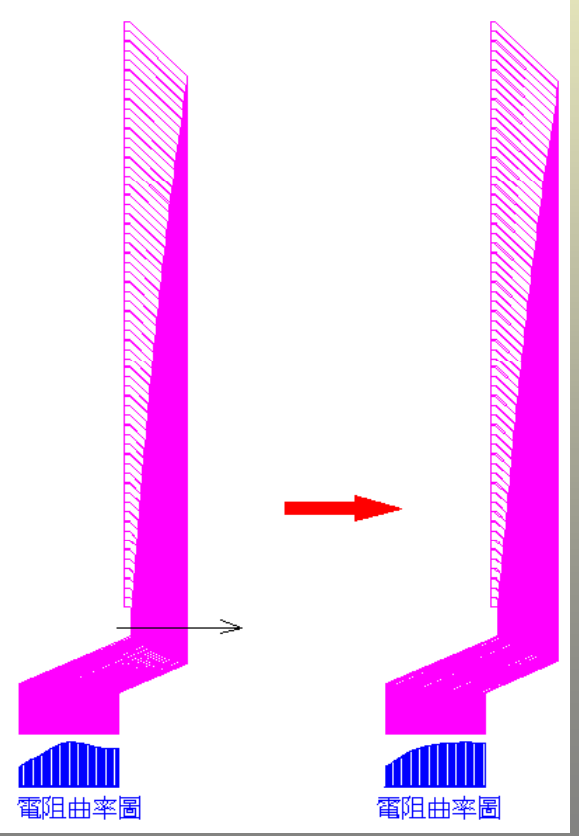
Width & Space adjustment (快速調整阻值均化作業)

1-1. +- 寬度值(for width)
1-2. 等差遞增/遞減
1-3. 等比遞增/遞減
1-4. 重新定義 min width & min space

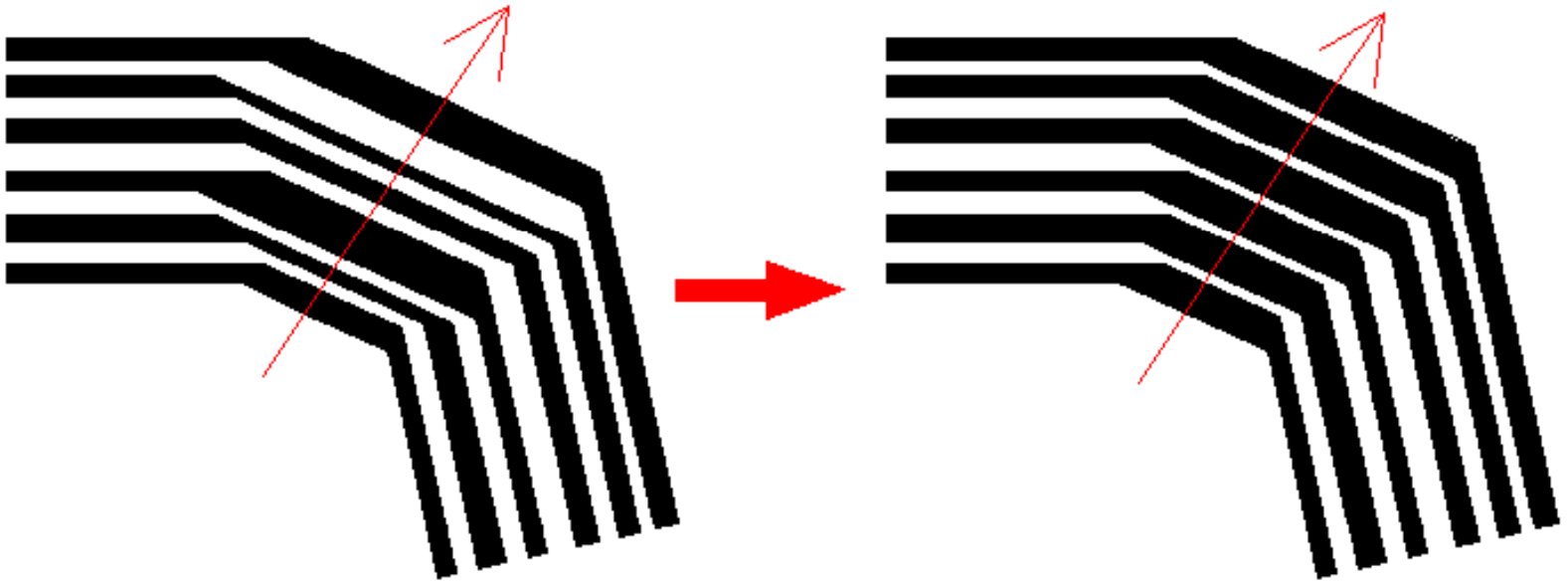
Width 為漸進式的遞增/減
Space 保持在 min-space



[調整案例]



(10-1). tarce width & space adjustment



將平行區段的電路重新安排 width 與 space

(11).

Drawing Chip and bump by Coordinates file

Microsoft Excel - BUMP_LIST.csv

檔案(F) 編輯(E) 檢視(V) 插入(I) 格式(O) 工具(T) 資料(D) 視窗(W) 說明(H)

Adobe PDF(B)

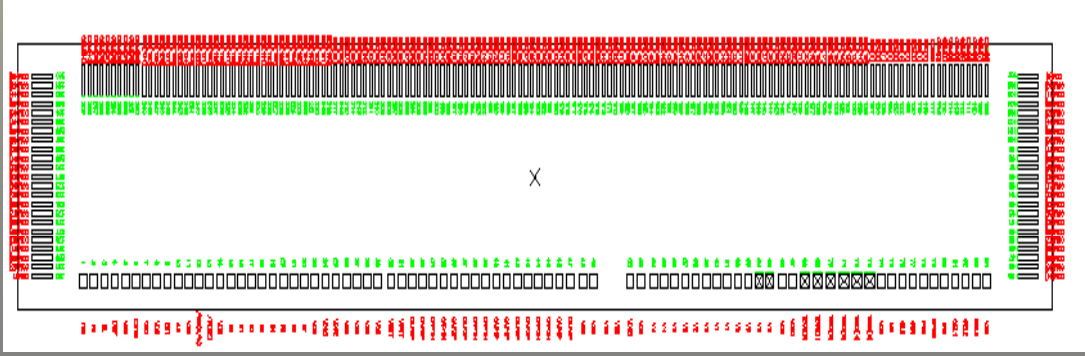
A1 BUMP_NO

	A	B	C	D	E	F
1	BUMP_NC	BUMP_NAM	X_COORD	Y_COORD	X_LEN	Y_LEN
2	1		66	4685.22	42	80.5
3	2		66	4491.22	42	50
4	3		66	4431.22	42	50
5	4		66	4204.36	42	50
6	5		66	4144.36	42	50
7			66	4074.86	42	50
8			66	3991.86	42	50
9	8		66	3876.36	42	50
10	9	VCC9	66	3816.36	42	50
11	10	VCC10	66	3714.03	42	50
12	11	VCC11	66	3654.03	42	50
13	12	VCC12	66	3594.03	42	50
14	13	VCC13	66	3534.03	60.3	50
15	14	VCC14	66	3474.03	60.3	60
16	15	VCC15	66	3414.03	60.3	45.5
17	16	VCC16	66	3354.03	60.3	45.5
18	17	VCC17	66	3294.03	60.3	45.5
19	18	VCC18	66	3234.03	60.3	45.5
20	19	VCC19	66	3174.03	60.3	45.5
21	20	VCC20	66	3114.03	60.3	45.5

BUMP_LIST

就緒

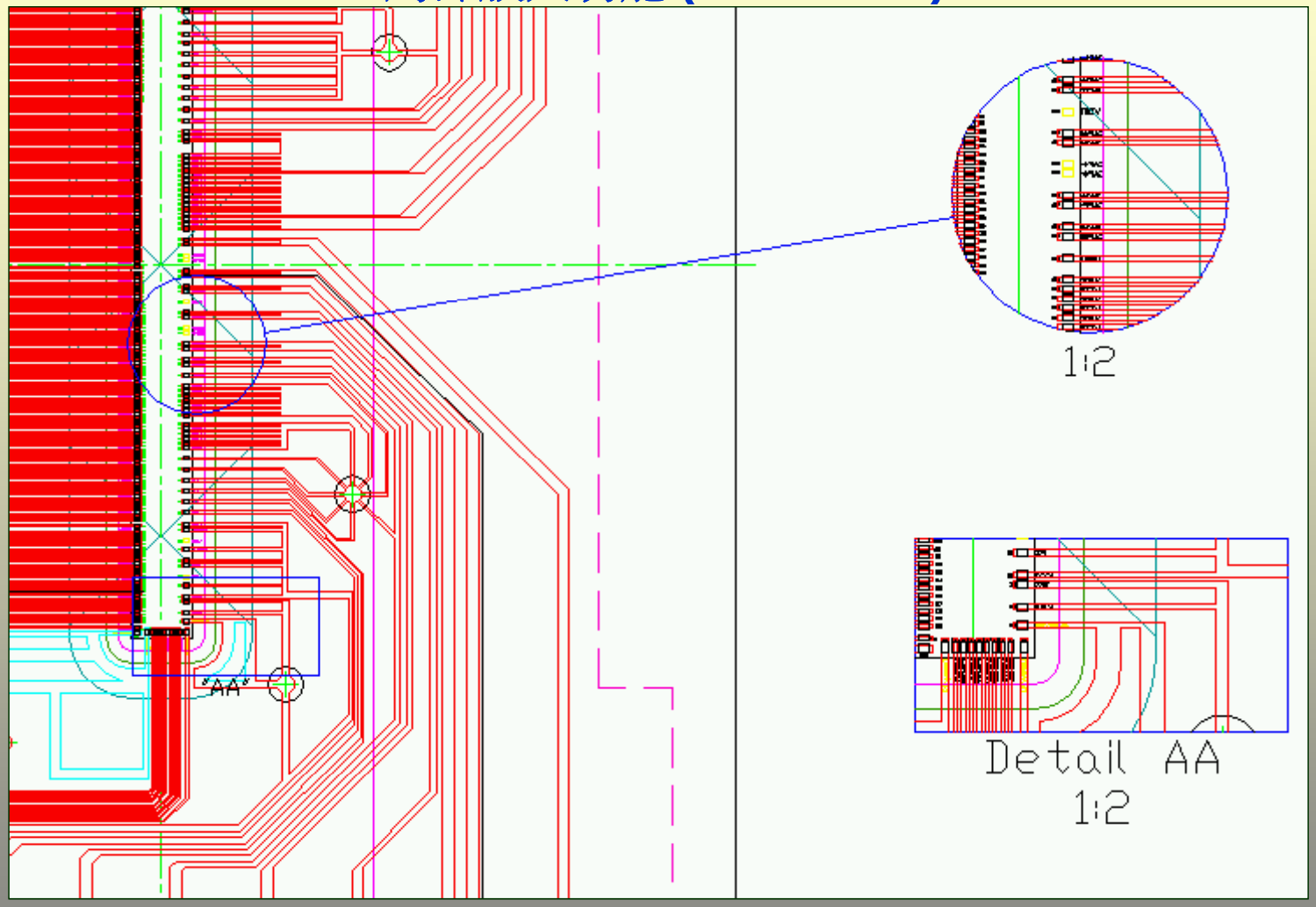
依座標檔自動繪出 chip/bump
bump no. / bump netname



(12).

Darwing detail view by define area

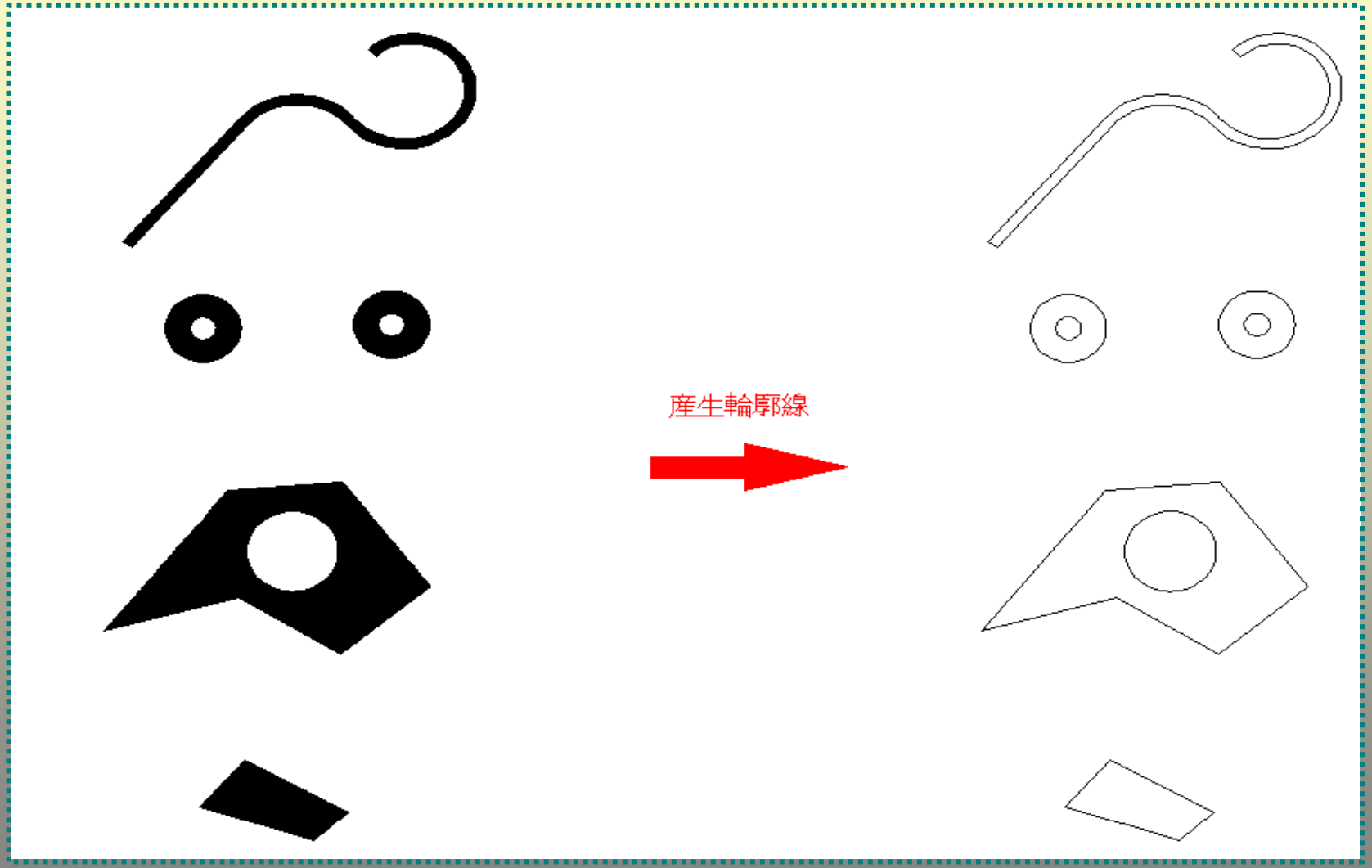
局部放大功能 **(detail view)**



放大範圍可為圓形與矩形

(13).

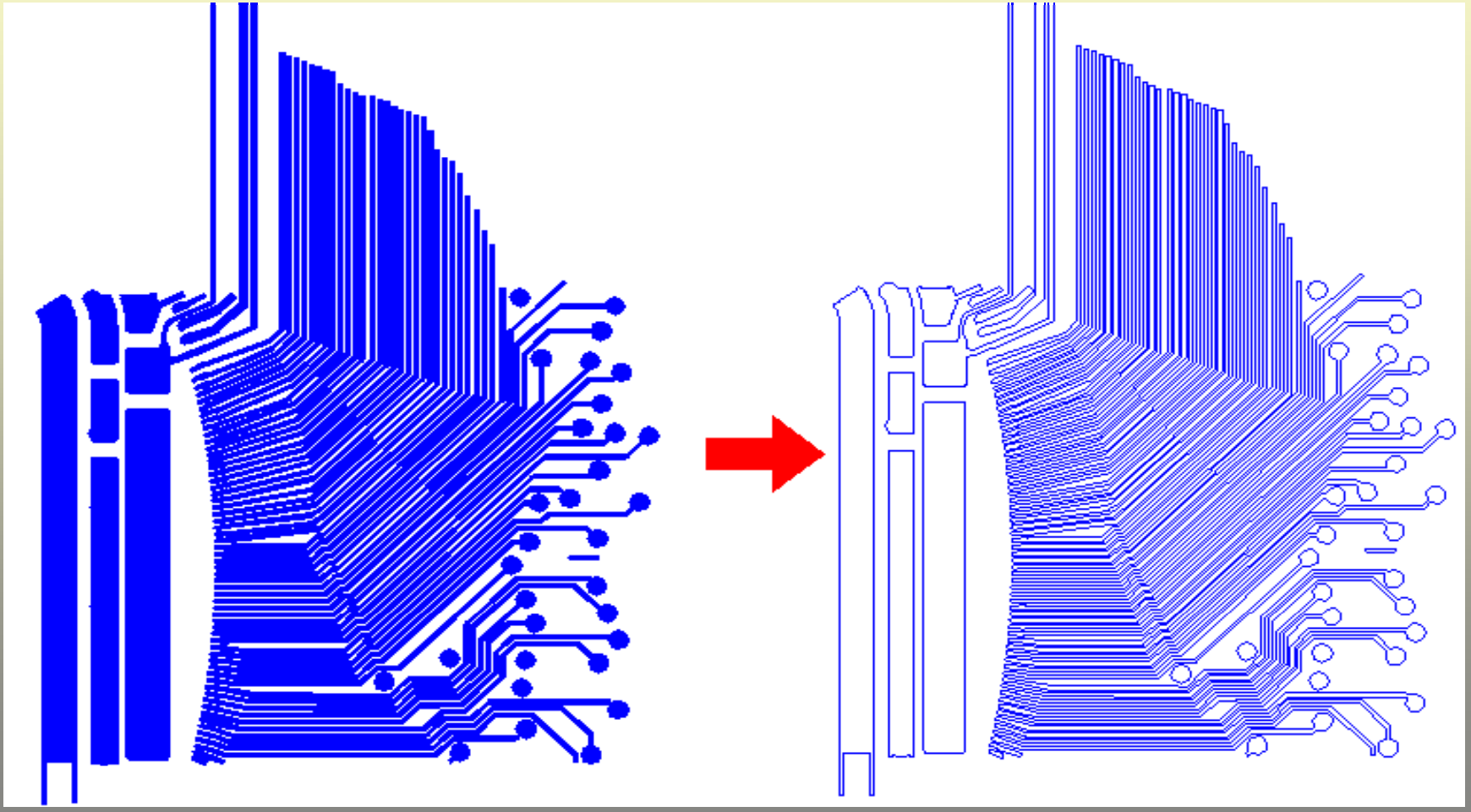
Generation object outline



(pline,solid,donut,hatch)

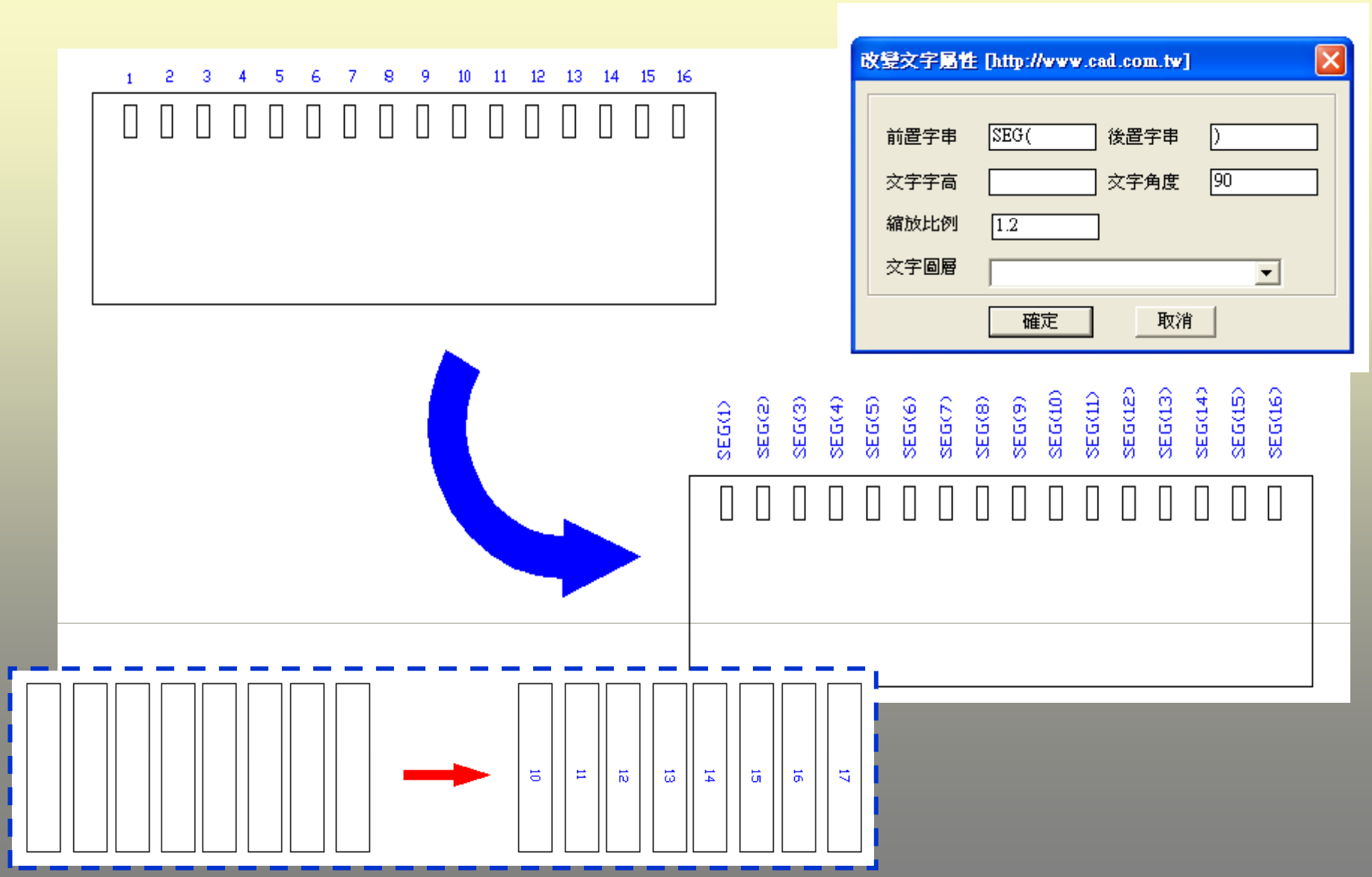
(13-1).

Auto generation electric circuit outline line



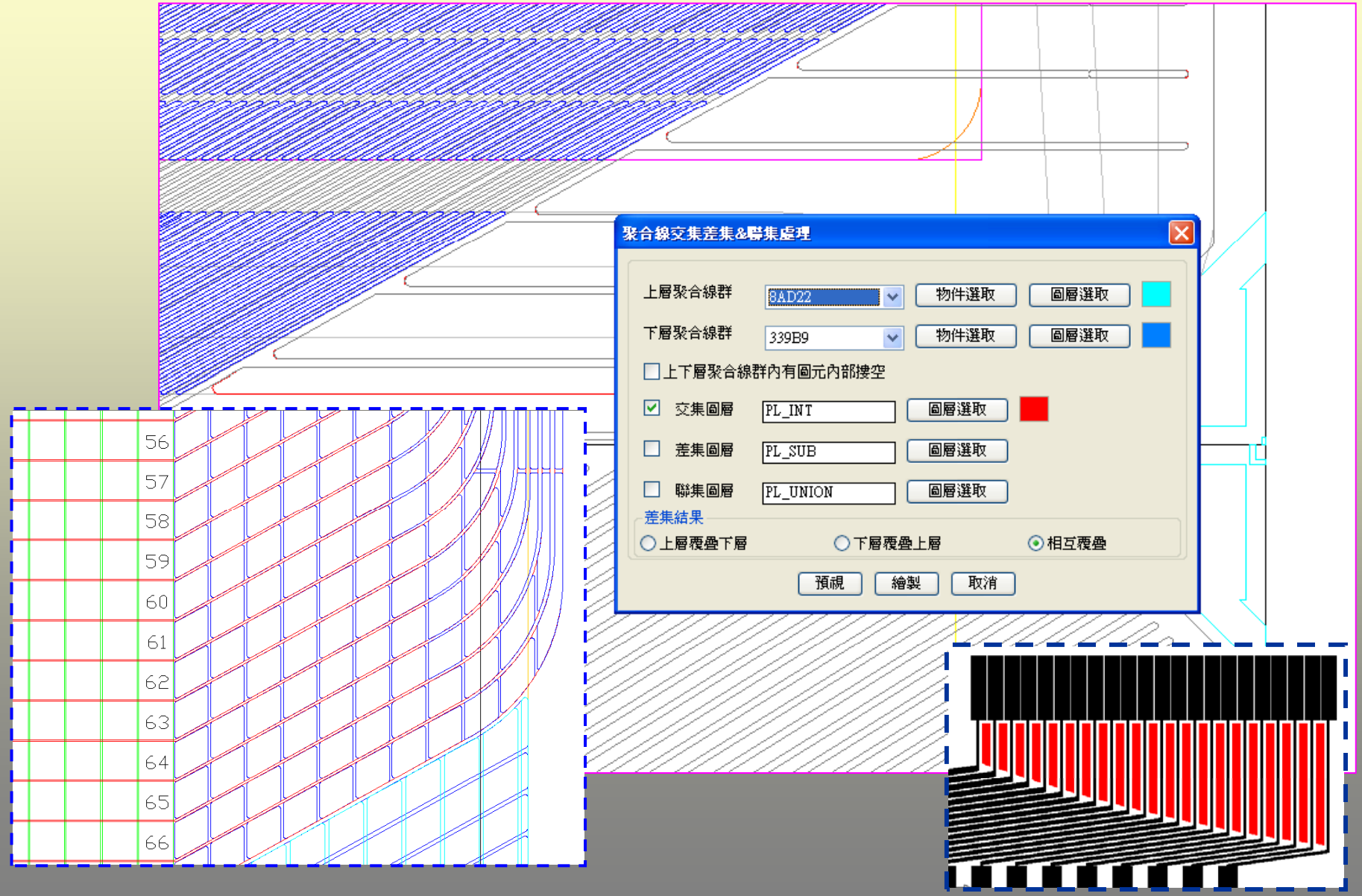
(14).

The text consecution serial number and attribute modify

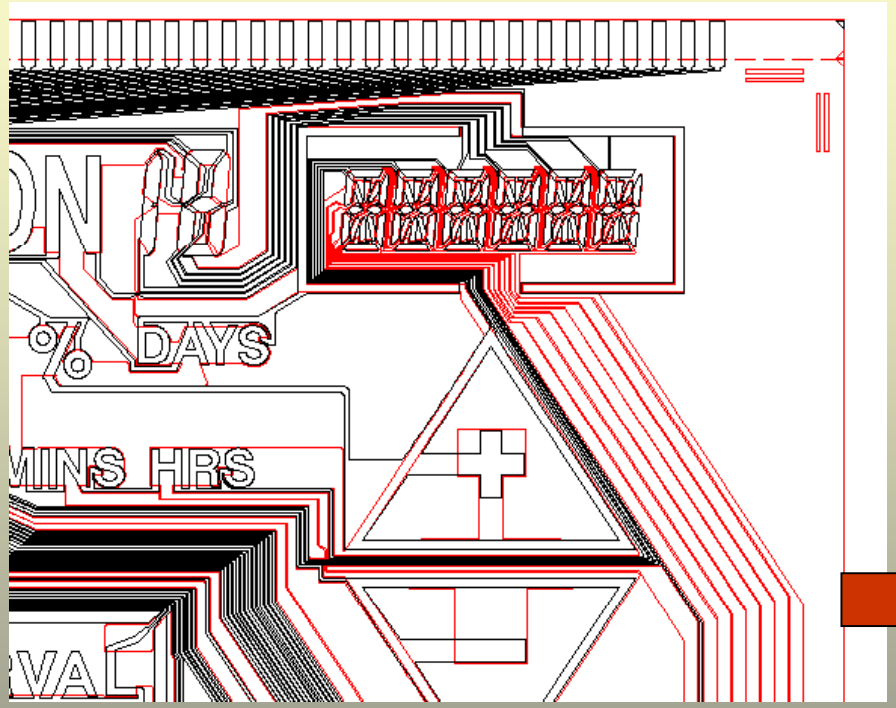


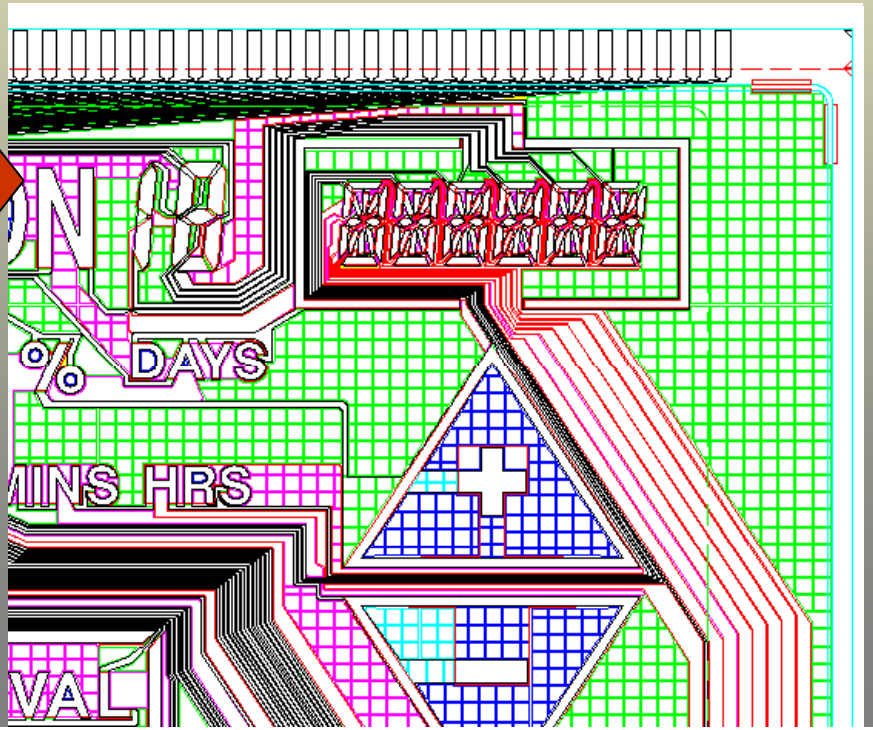
(15).

Dummy trace design automatically



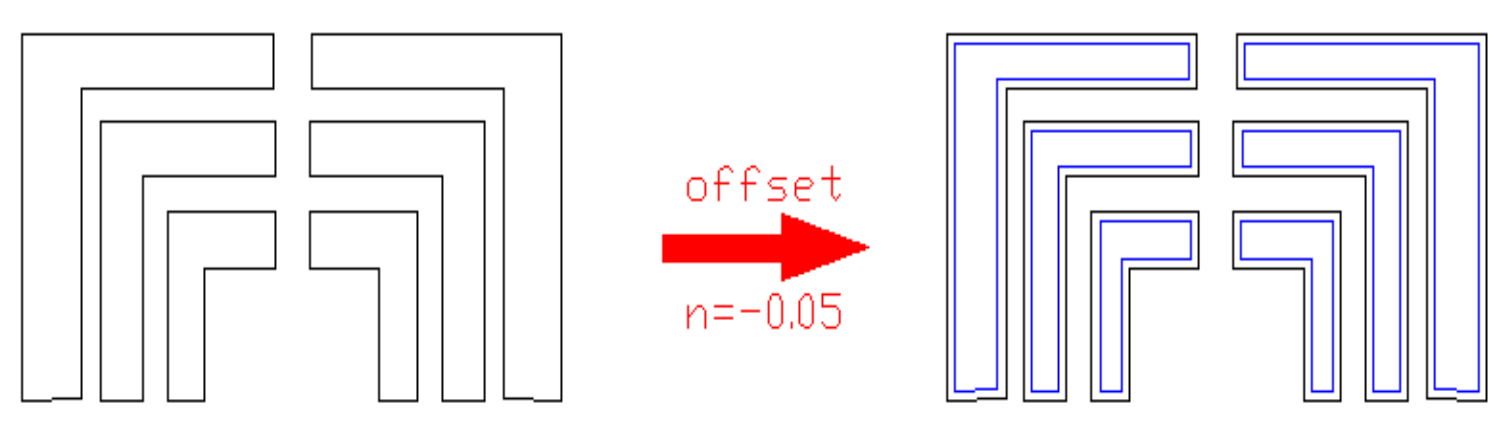
Auto draw to repair box dummy

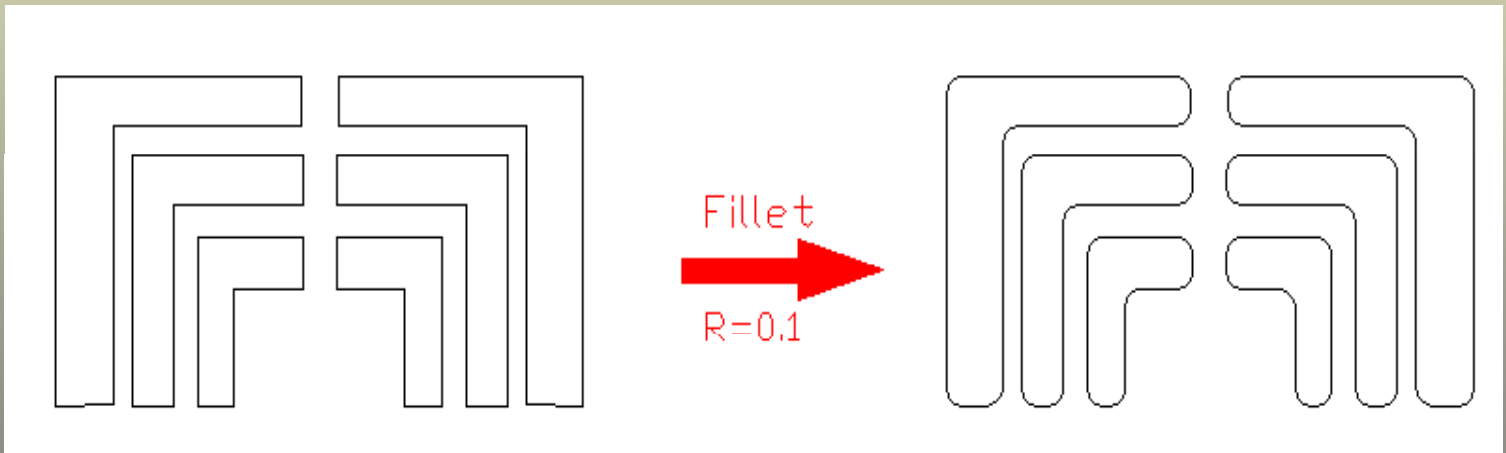




(15).

The whole offset and fillet



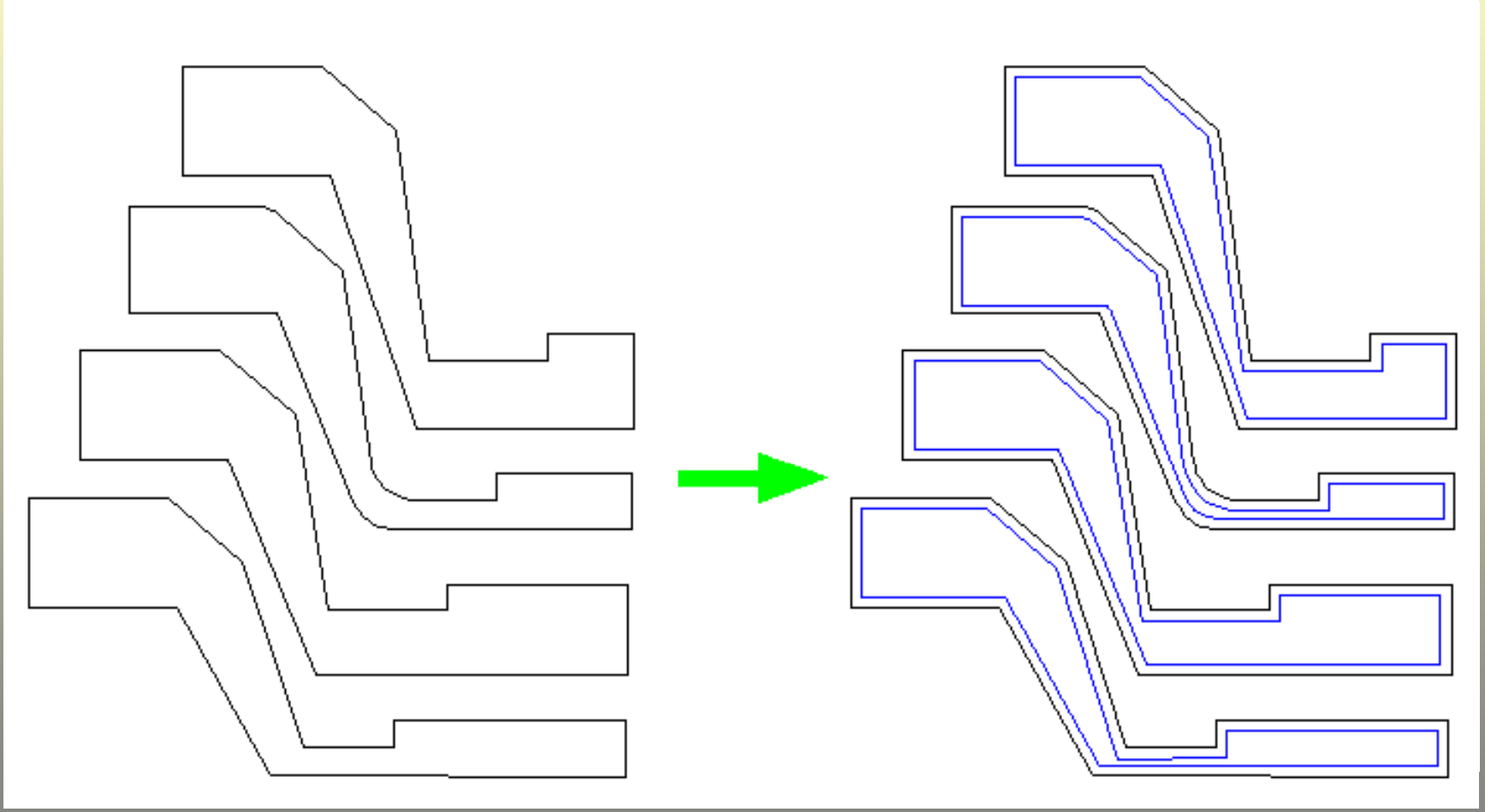


(After canning choose much a processing)

(15-1).

Close pline whole do offset

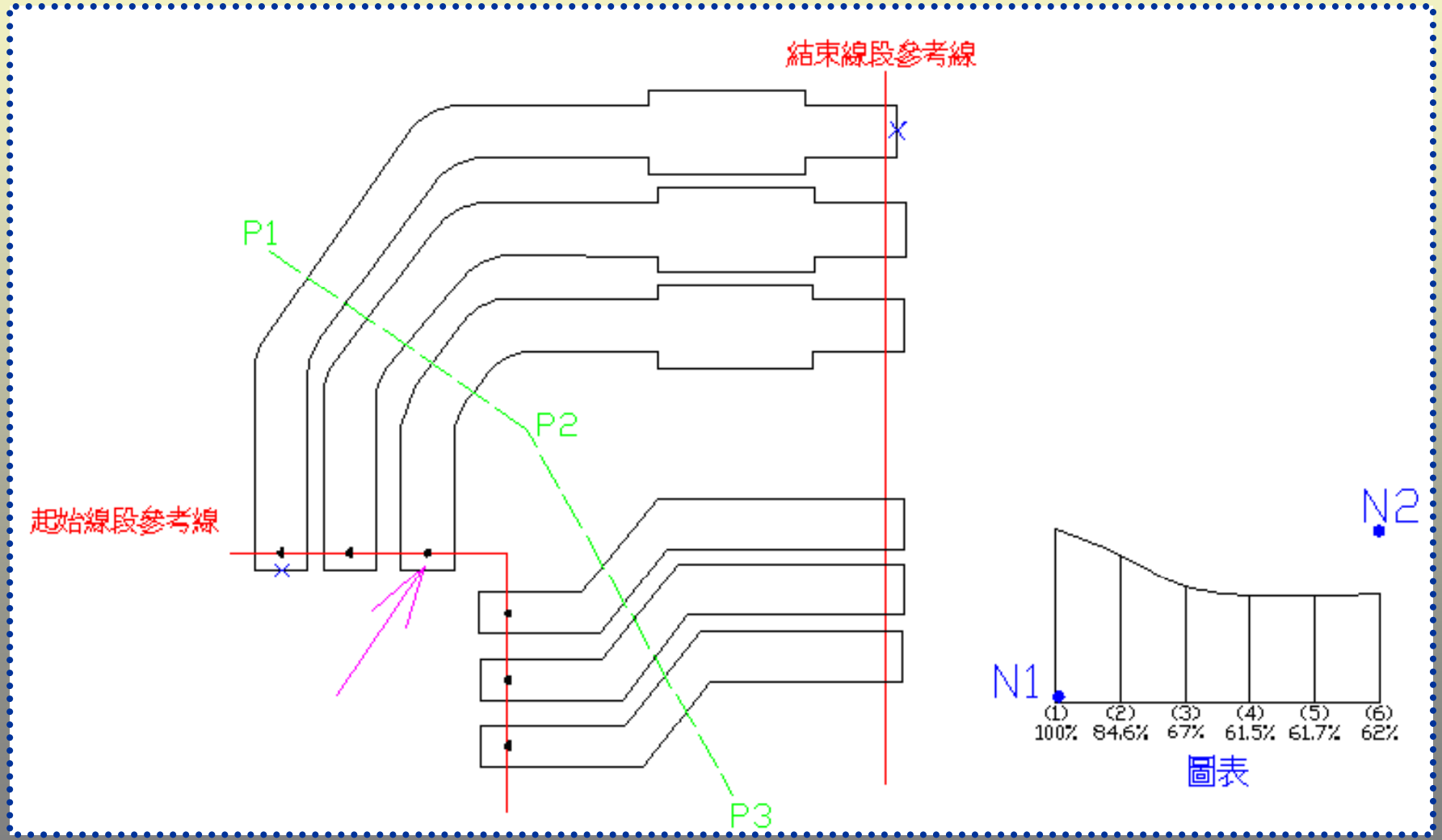
(Can go toward outside or go toward inside)



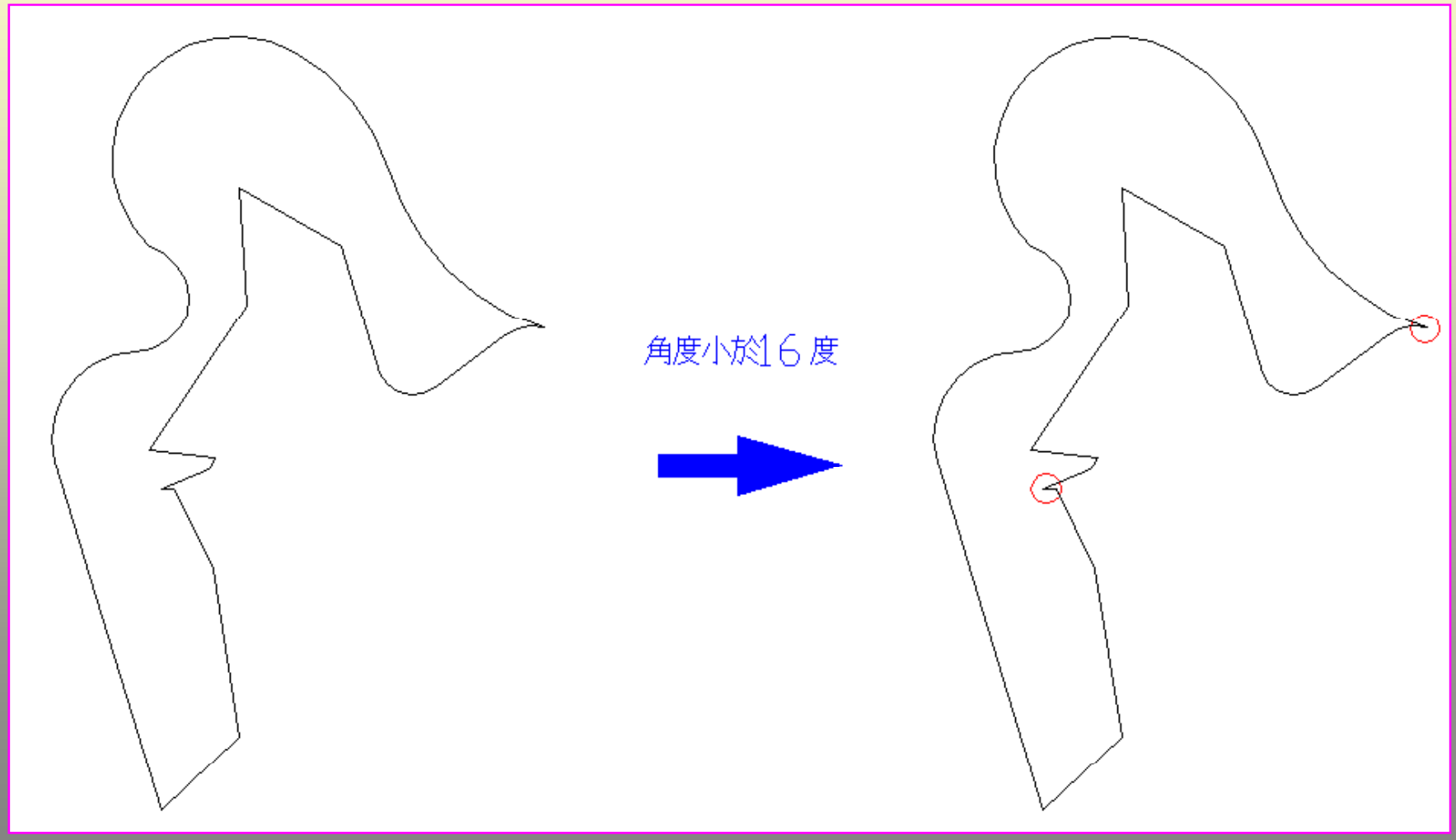
(貳)

LCD ITO trace checking and Analysis

(1). **Resistance analysis :**

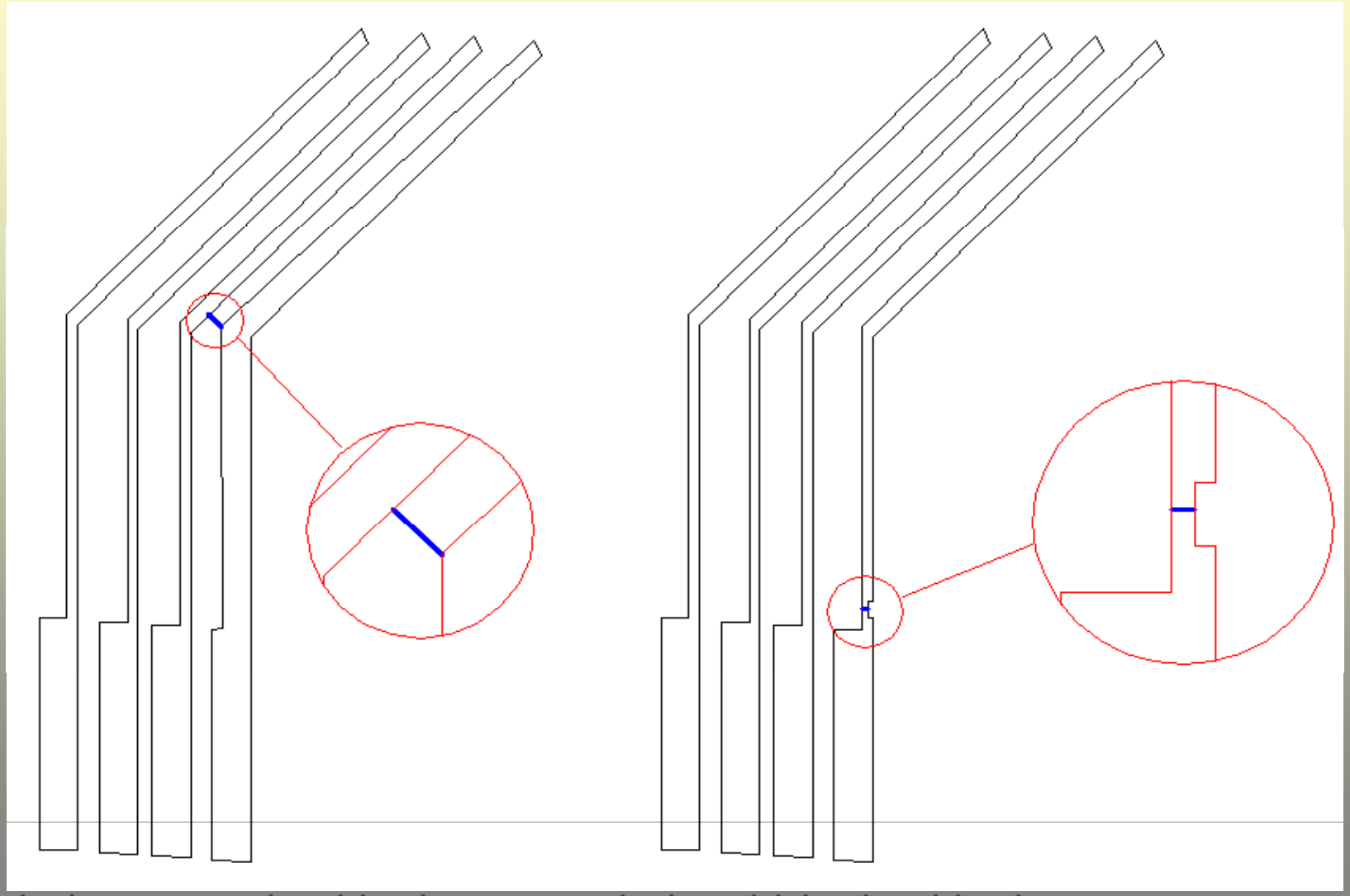


(2). **Check the turning of the electric circuit absurdity corn, examine for the convenience of the quality of the electric circuit**



(3).

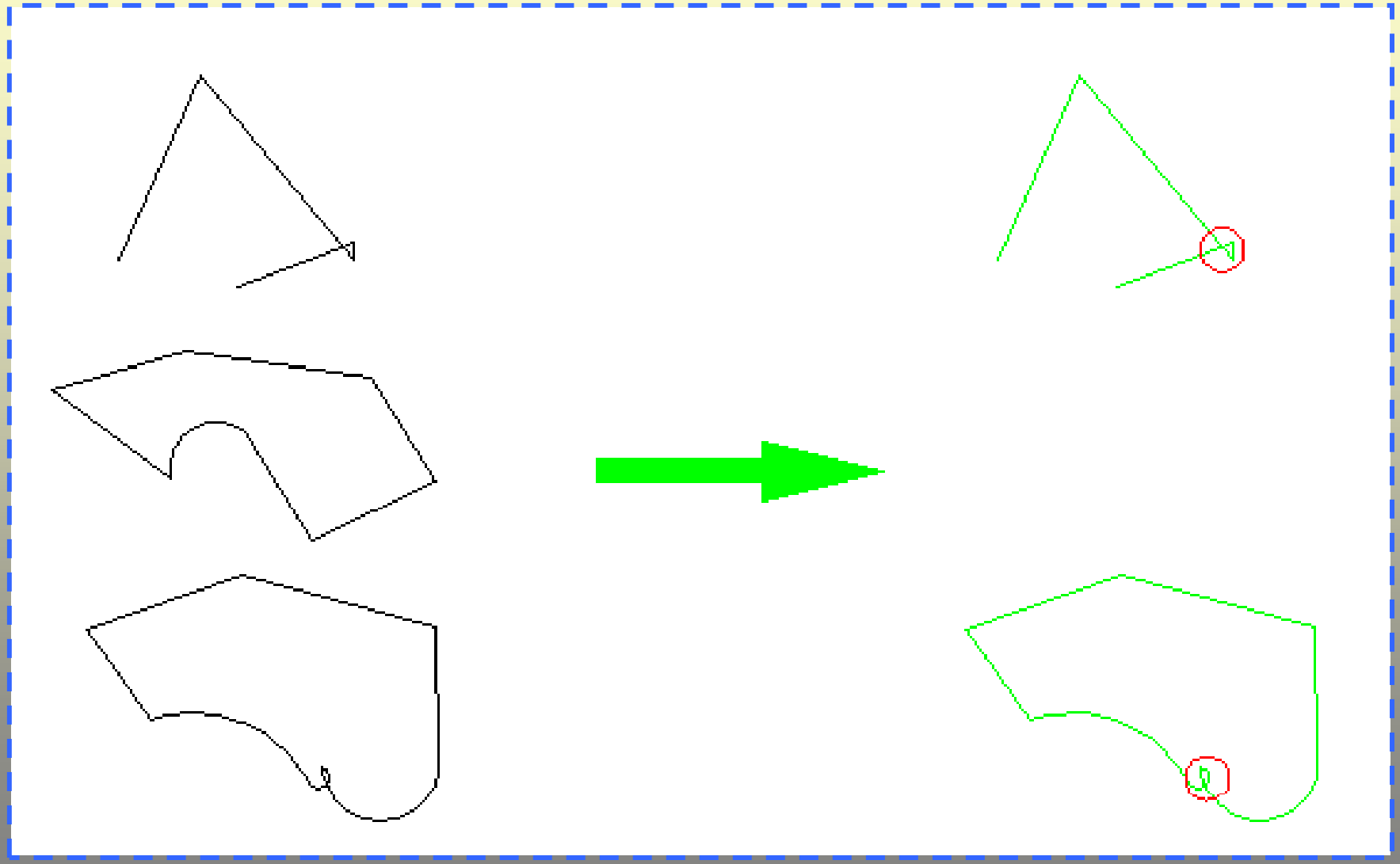
自動檢查 min width 與 min space



(min space checking)

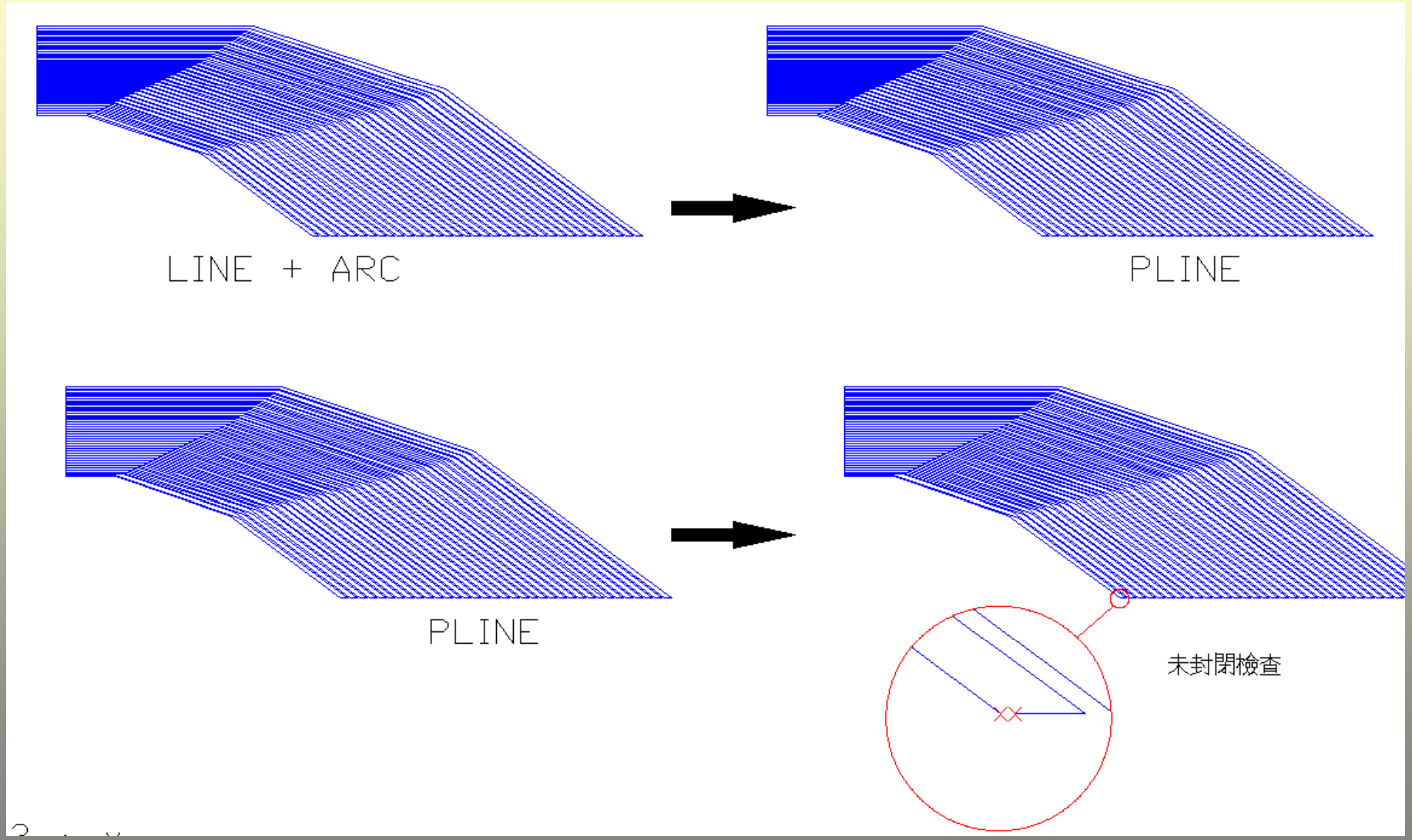
(min width checking)

(4). Checking crossing trace(closed pline)



(5).

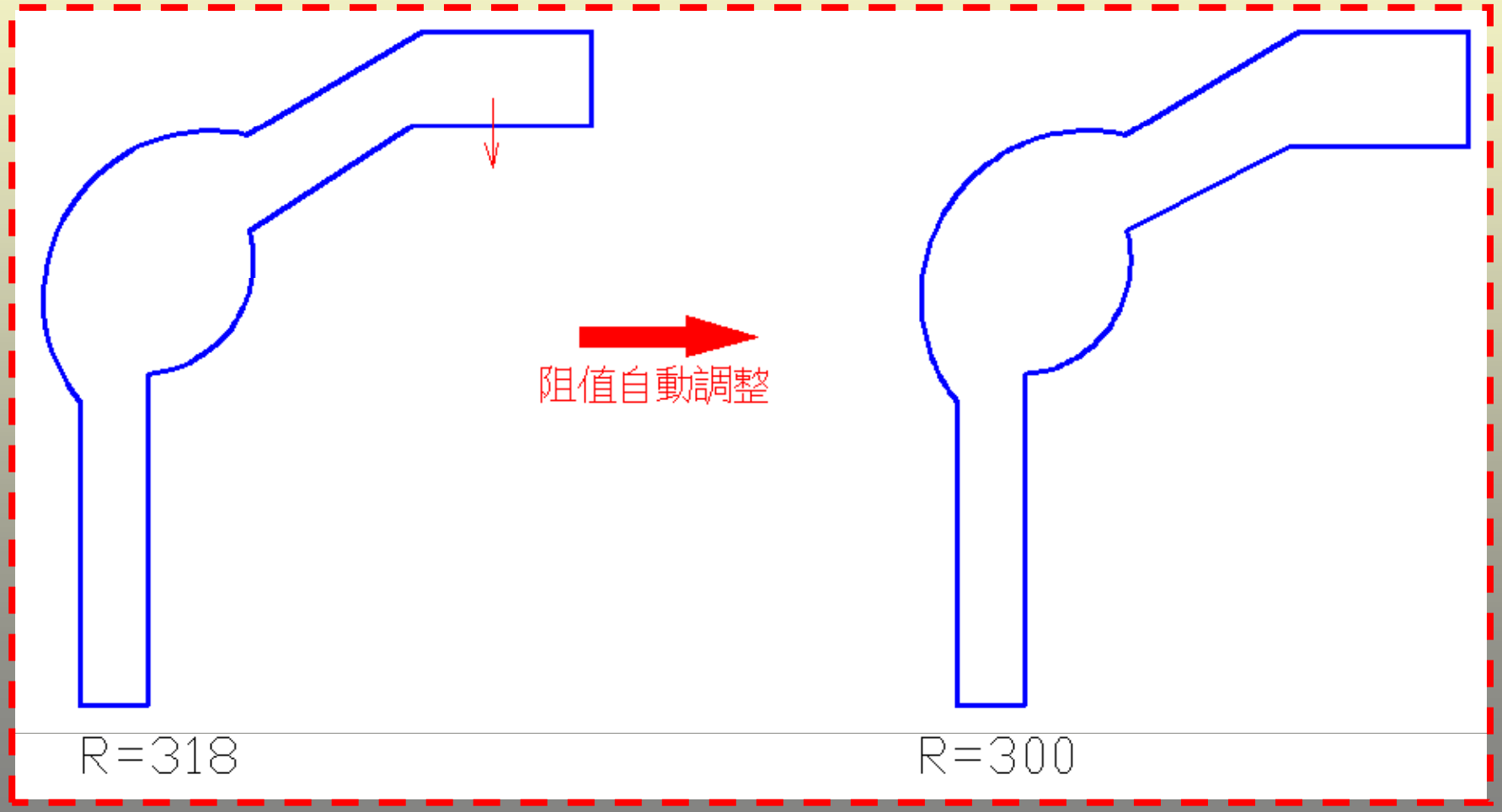
Checking the open trace and show the broken location



(6).

Adjust the trace to fit resistance

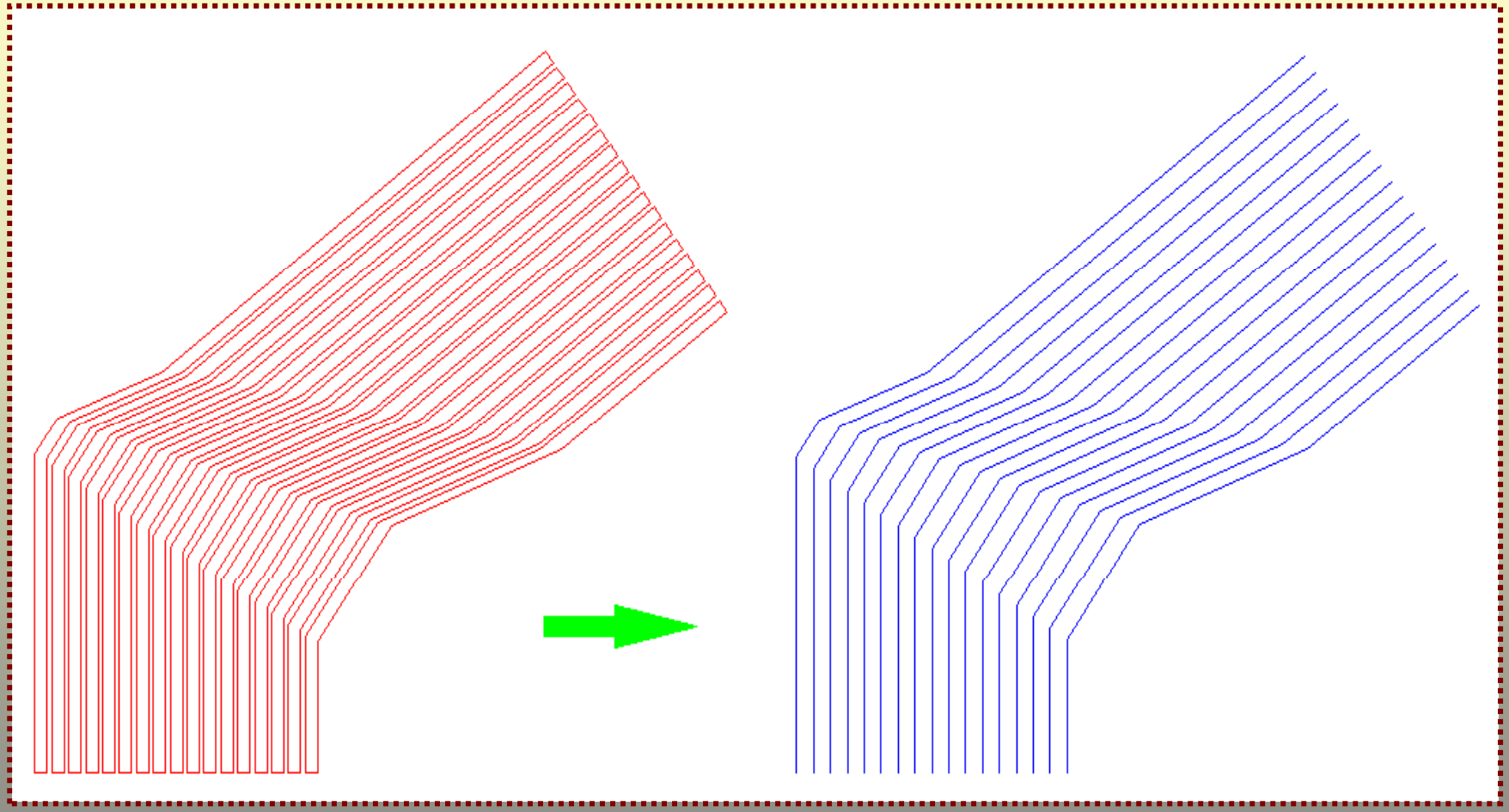
輸入該 **tarce** 期望之阻值,由系統自動調整寬度至最佳化位置



(自動改變邊界線位置以利阻值的調整)

(7).

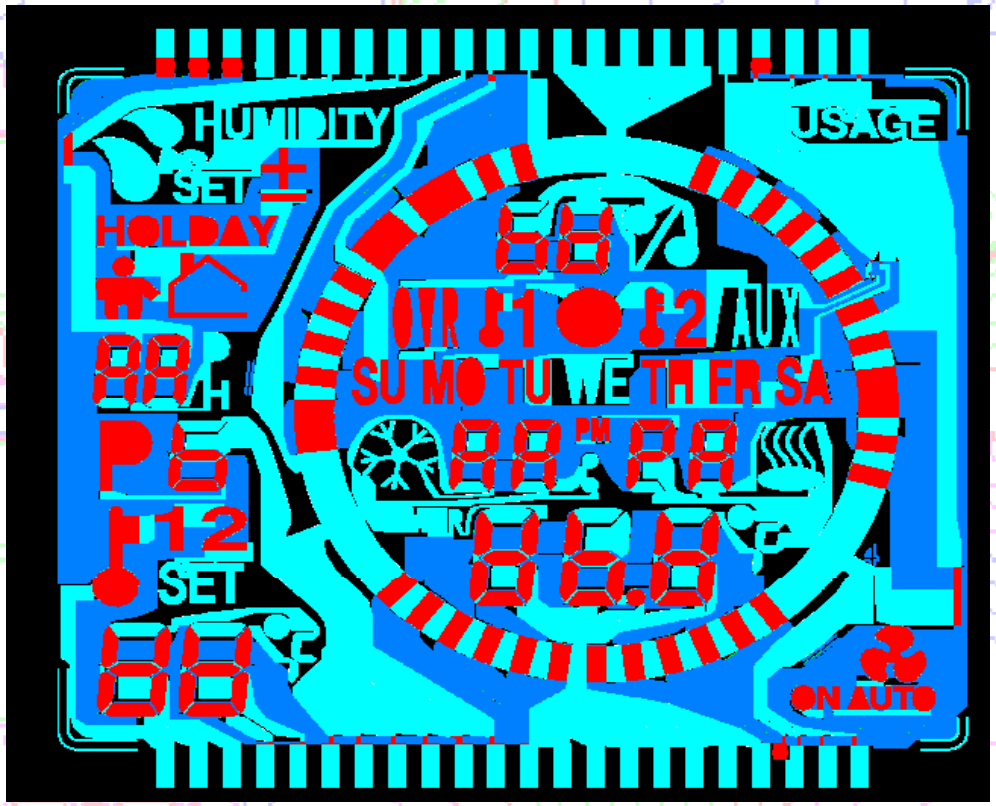
Generate the center line of trace



自動產生 **trace (電路)**的中心線圖

(8).

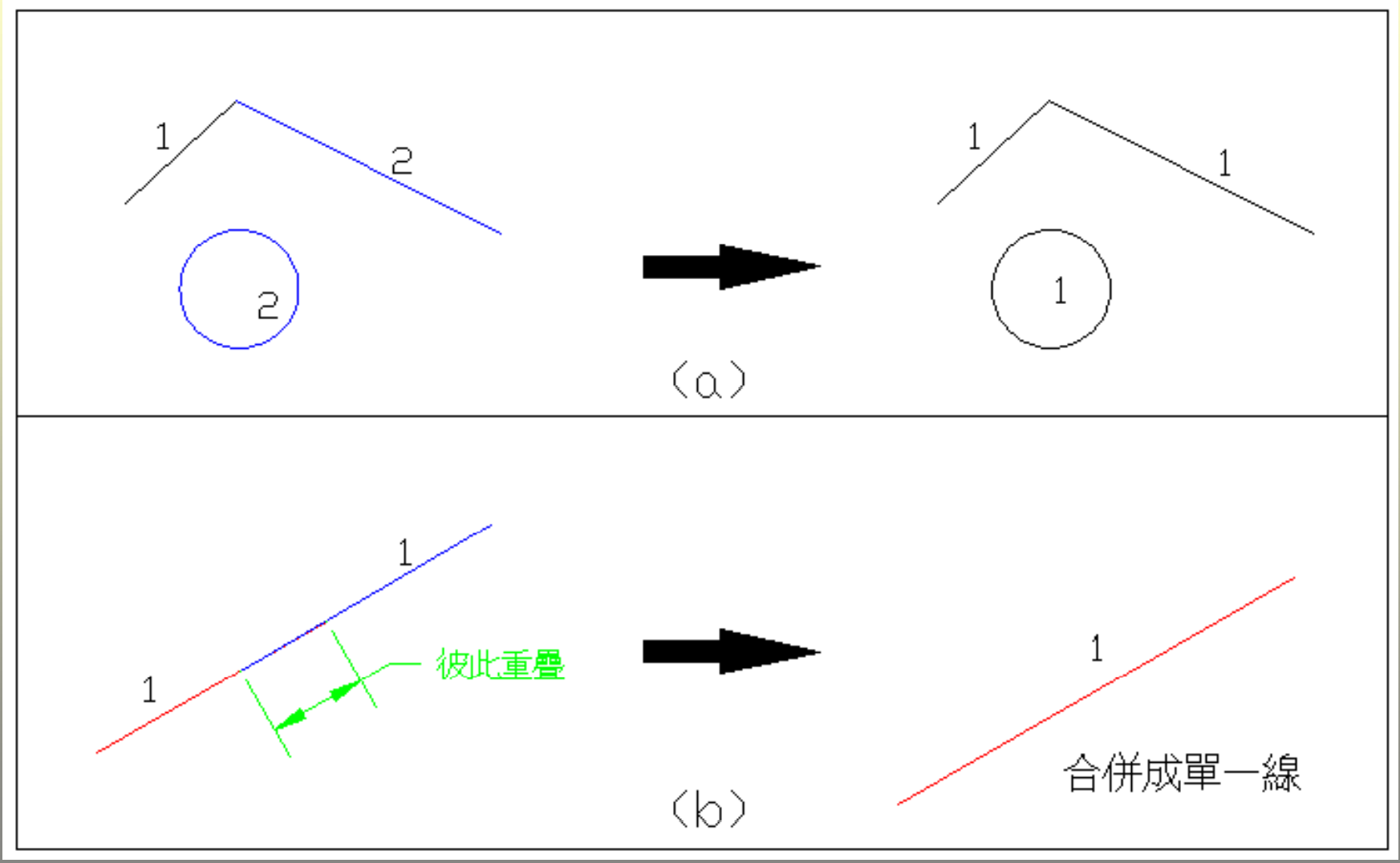
Preview the result



(紅色區域為點亮區)

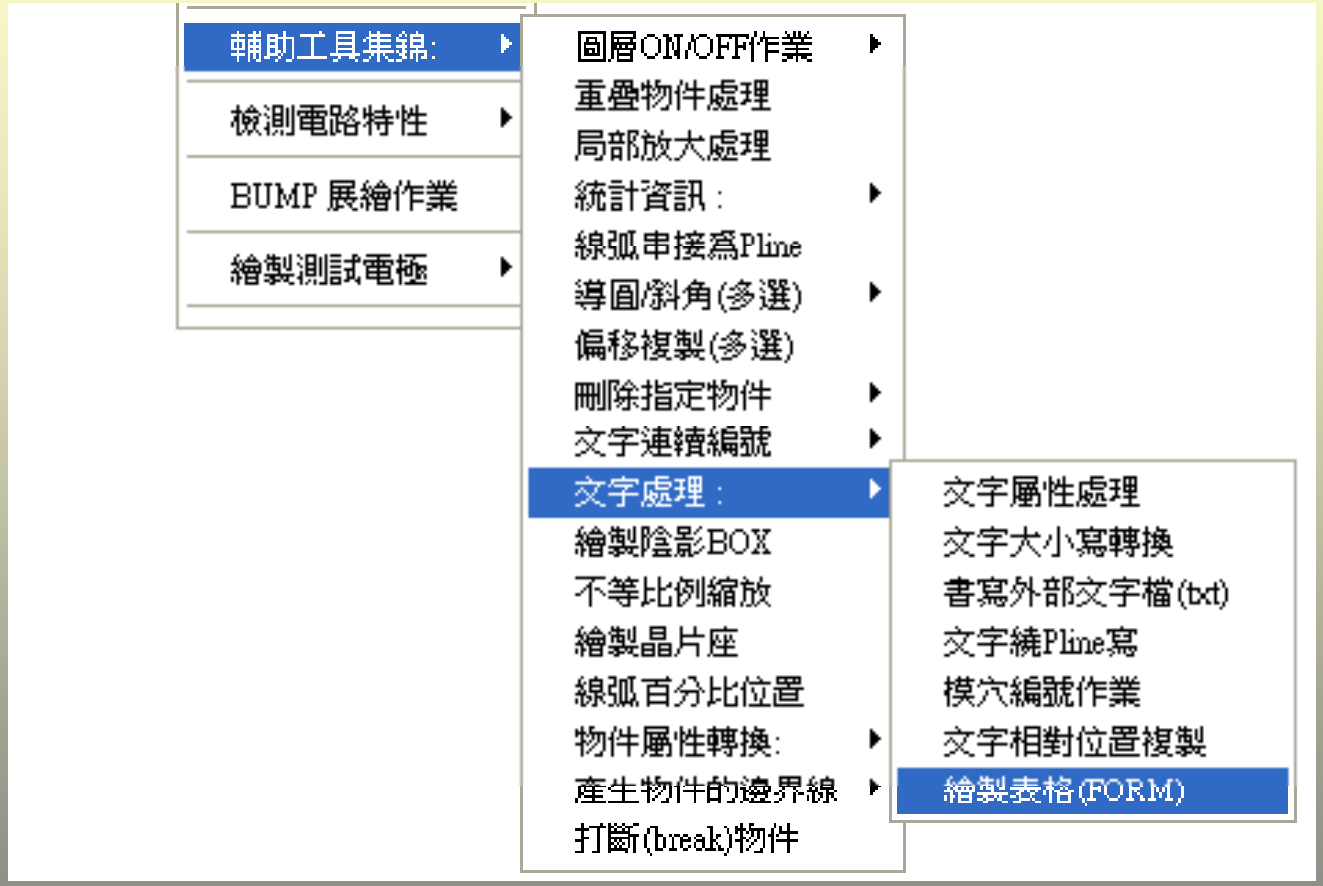
(9).

Delete layer after layer object with whole combine to hand over to fold line



Insures the Pline object that the electric circuit can be single closing

(參)
LCD ITO electric circuit support design tools



Support design tools :

(1). Read into the exterior text file

(2). Delete particular object

(3).統計數量與線長

(4).不等比例縮放

(5).Diagram layer On/Off

(6).文字相對位置複製

(5). 一次倒斜角

(6). 物件打斷

(7). 表格快速繪製

(8). 電路曲折繪製

(9). 模穴快速編號

(10). 面積統計

(11). 繪製間格線

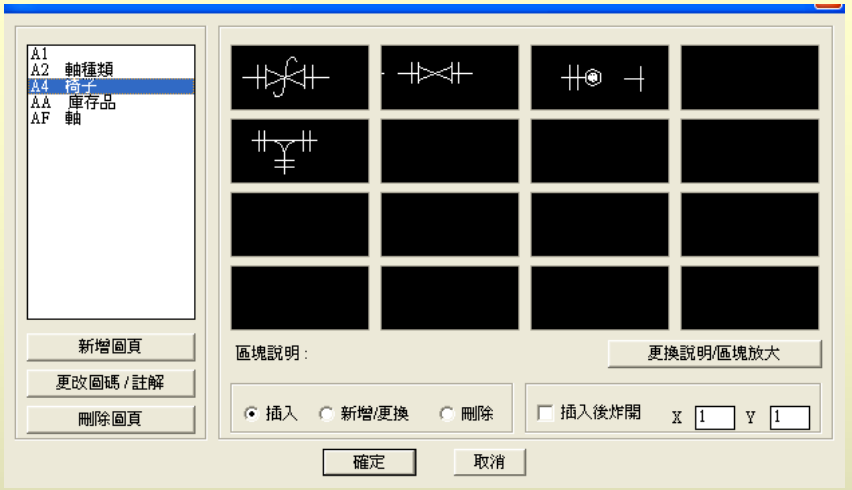
(12). 線弧百分比位置

(13). 中英文詞庫管理

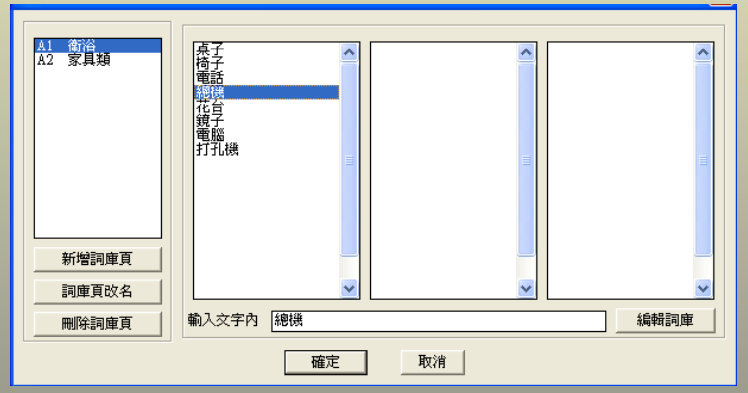
(14). 圖庫(block)管理

(15). 刪除長度為零的線段

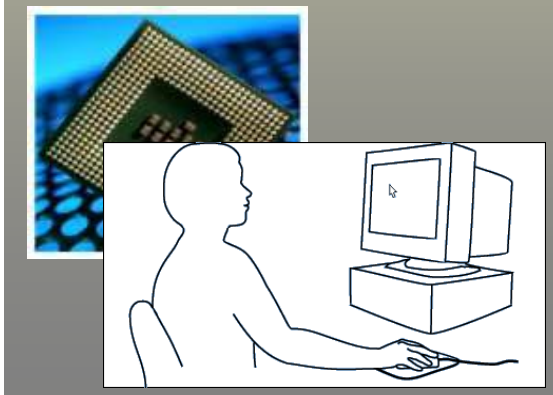
……etc.



(圖庫管理)

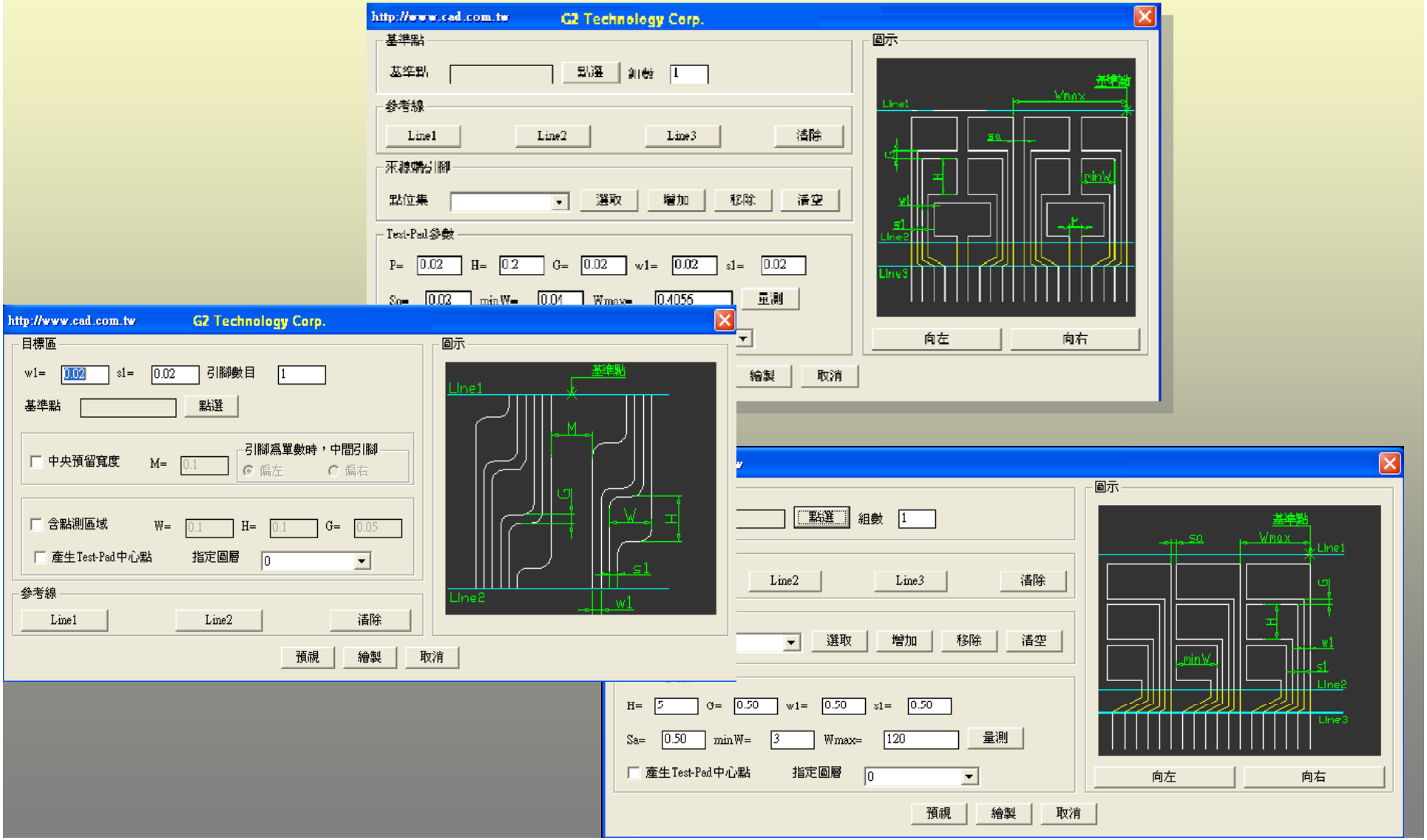


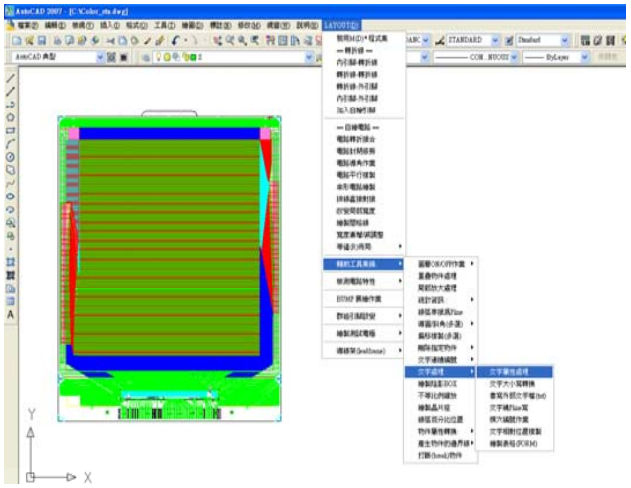
(中英文詞庫管理)



(肆)

FPC / COF testpad drawing





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