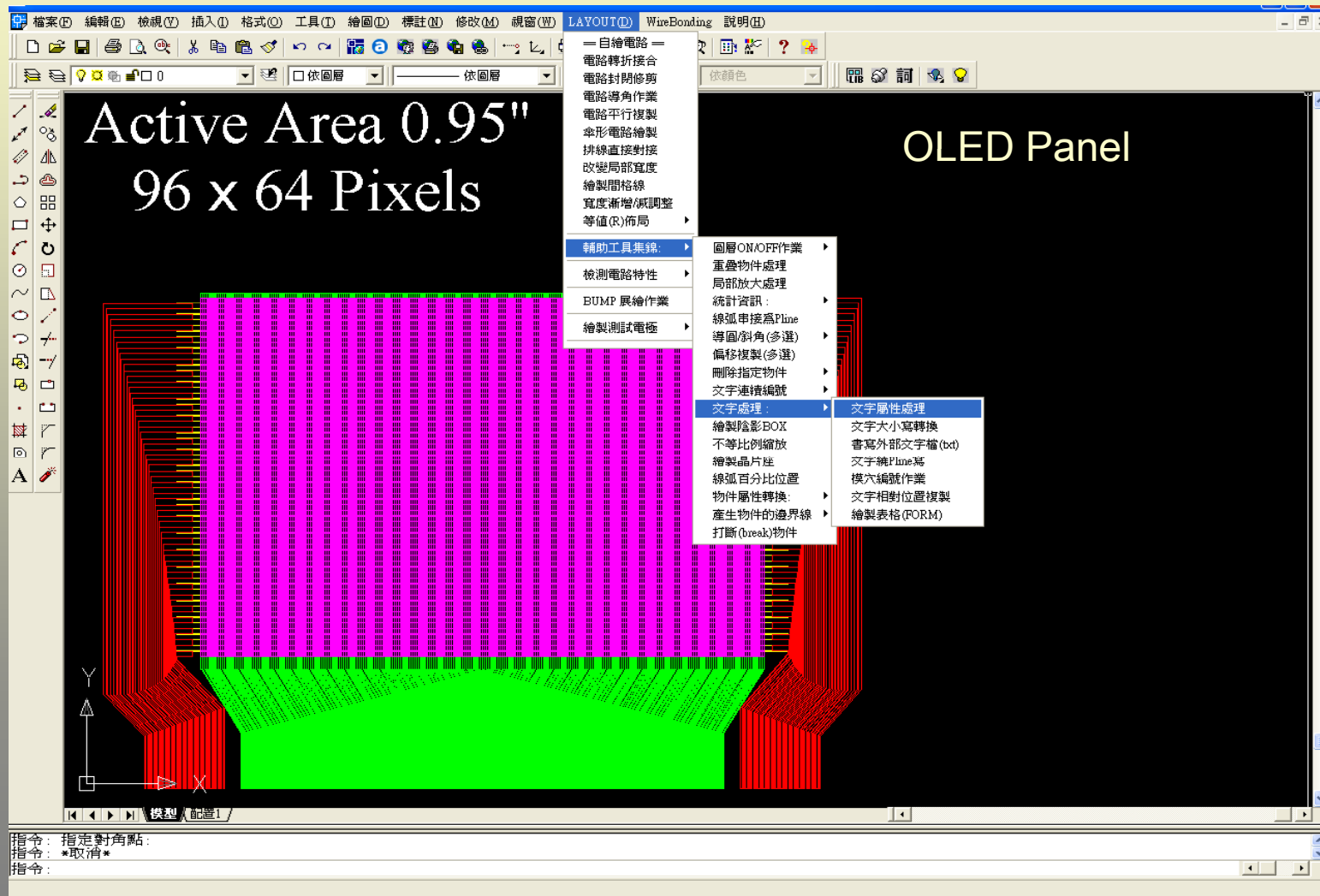


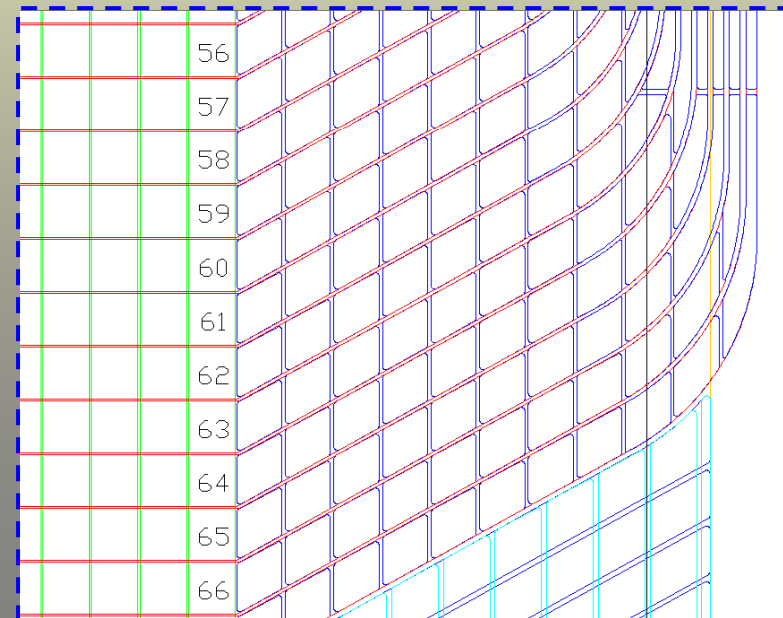
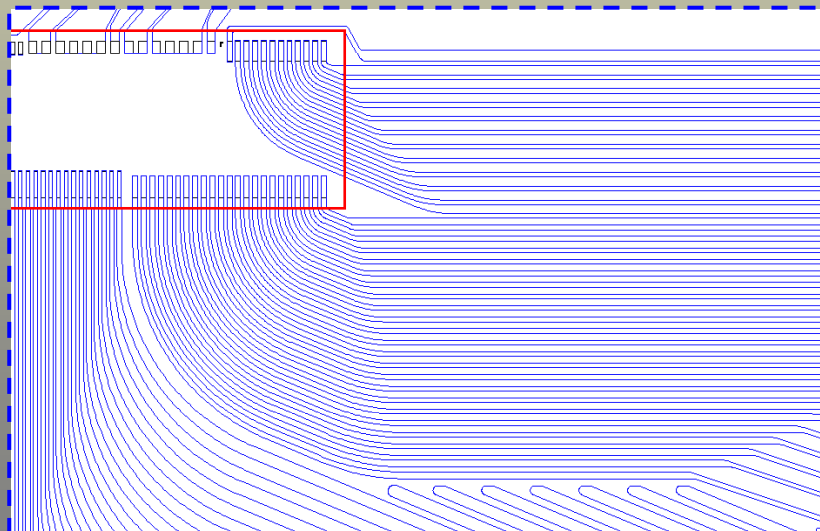
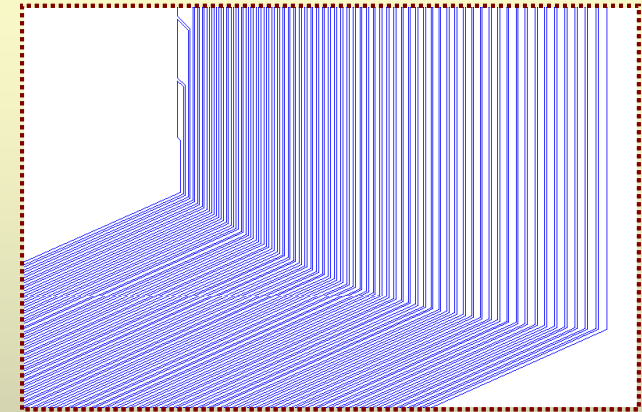
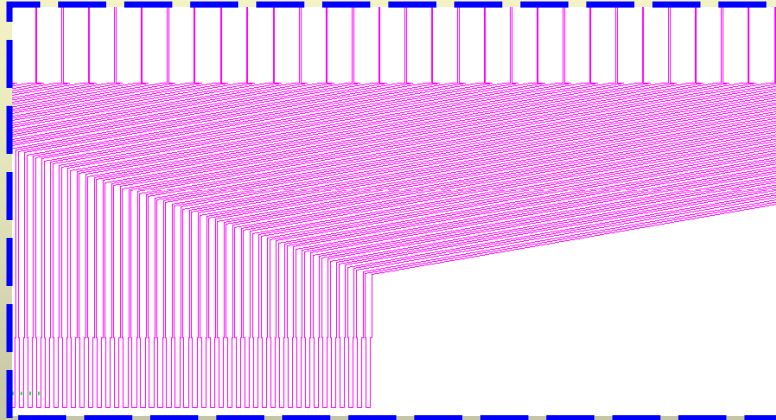
Gtools ITO trace layout & checking tools

(for AutoCAD based)

1. Electric circuit support to layout
2. Electric circuit examination and adjustment
3. support to facilities tool collections

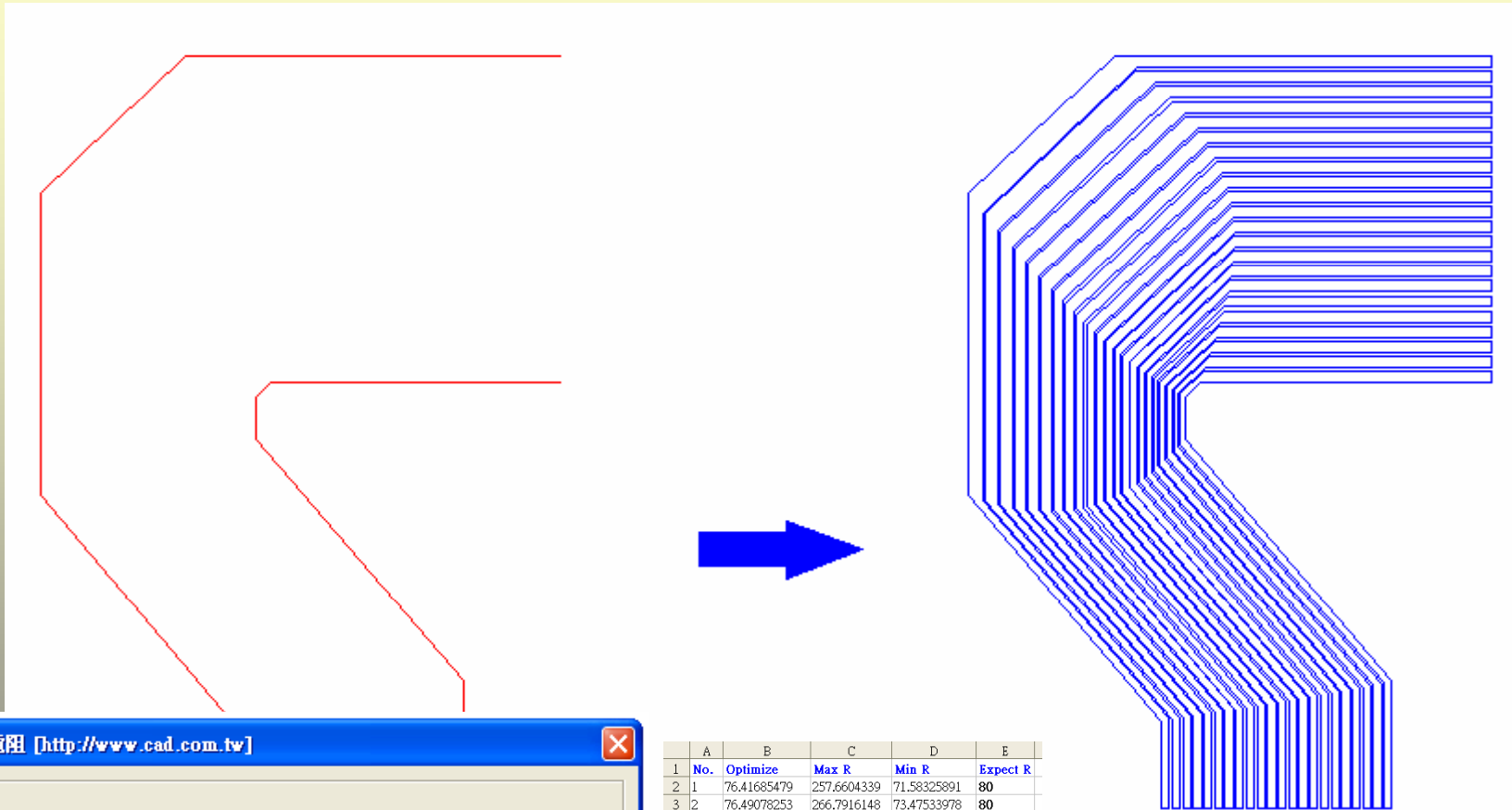


(壹) CSTN/STN LCD/OLED ITO electric circuit support to layout



(1). In the scope equal electric resistance auto layout

Within the scope of limited space, auto layout the optimization R(equal R), can also be worth in the R of appointed each electric circuit inside the excel



範圍內等電阻 [http://www.cad.com.tw]

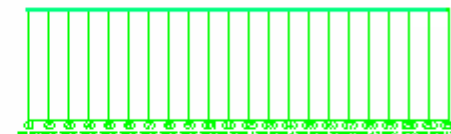
最小寬度 最小間隙 數量

固定 起始端寬度 封閉

固定 終止端寬度 封閉

自訂阻值

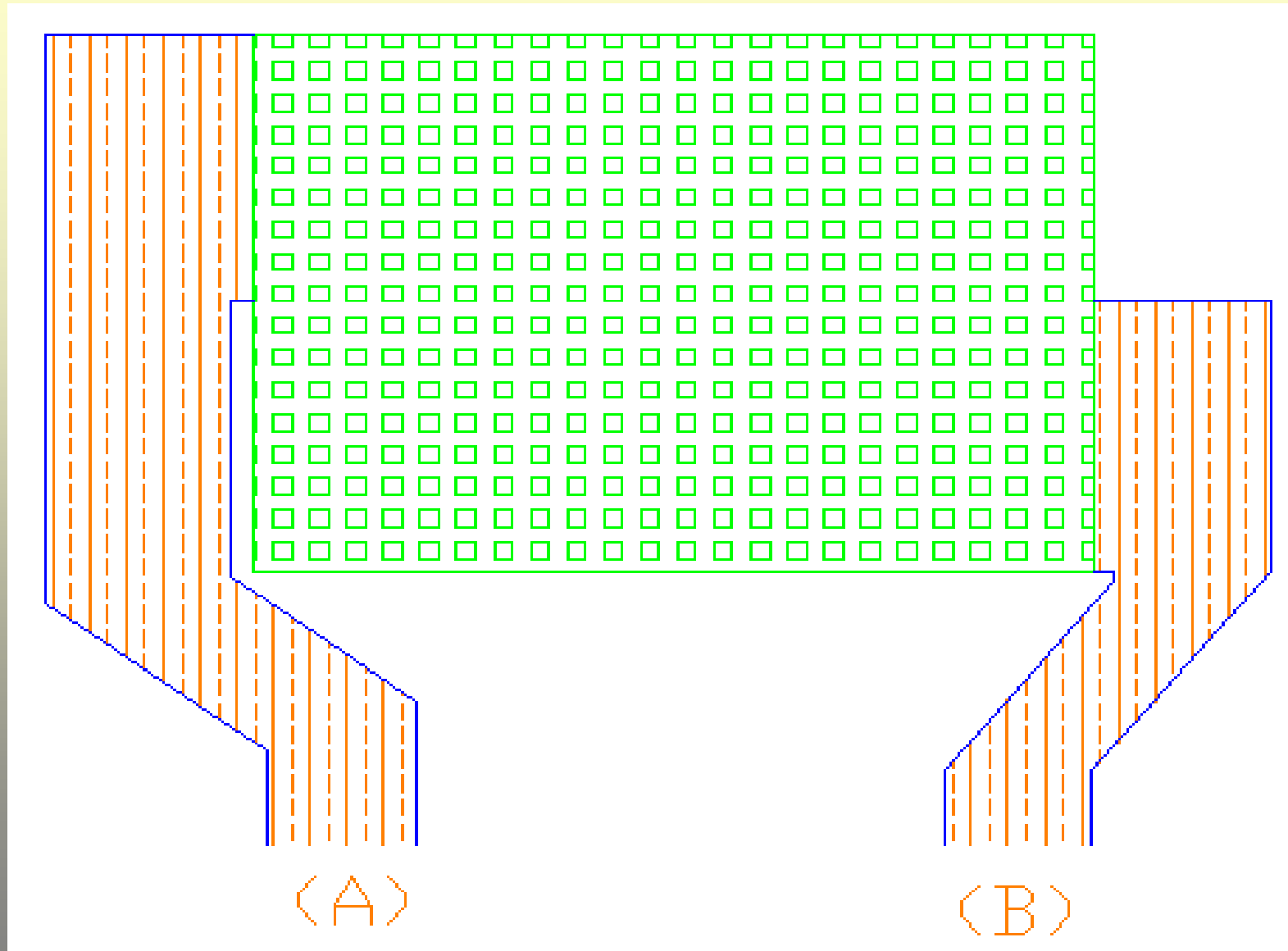
	A	B	C	D	E
1	No.	Optimize	Max R	Min R	Expect R
2	1	76.41685479	257.6604339	71.58325891	80
3	2	76.49078253	266.7916148	73.47533978	80
4	3	76.49078253	274.0953752	74.88740229	90
5	4	76.49078253	281.6875444	75.82067623	90
6	5	76.49078253	289.6642584	76.32624772	95
7	6	76.49078253	298.1216535	76.49078253	95
8	7	76.49078253	307.155866	76.41961945	100
9	8	76.49078253	316.8630321	76.2217803	100
10	9	76.49078253	327.339288	75.99880139	90
11	10	76.50009644	343.0798345	75.83703277	90



(common area autolayout) 阻值曲率圖

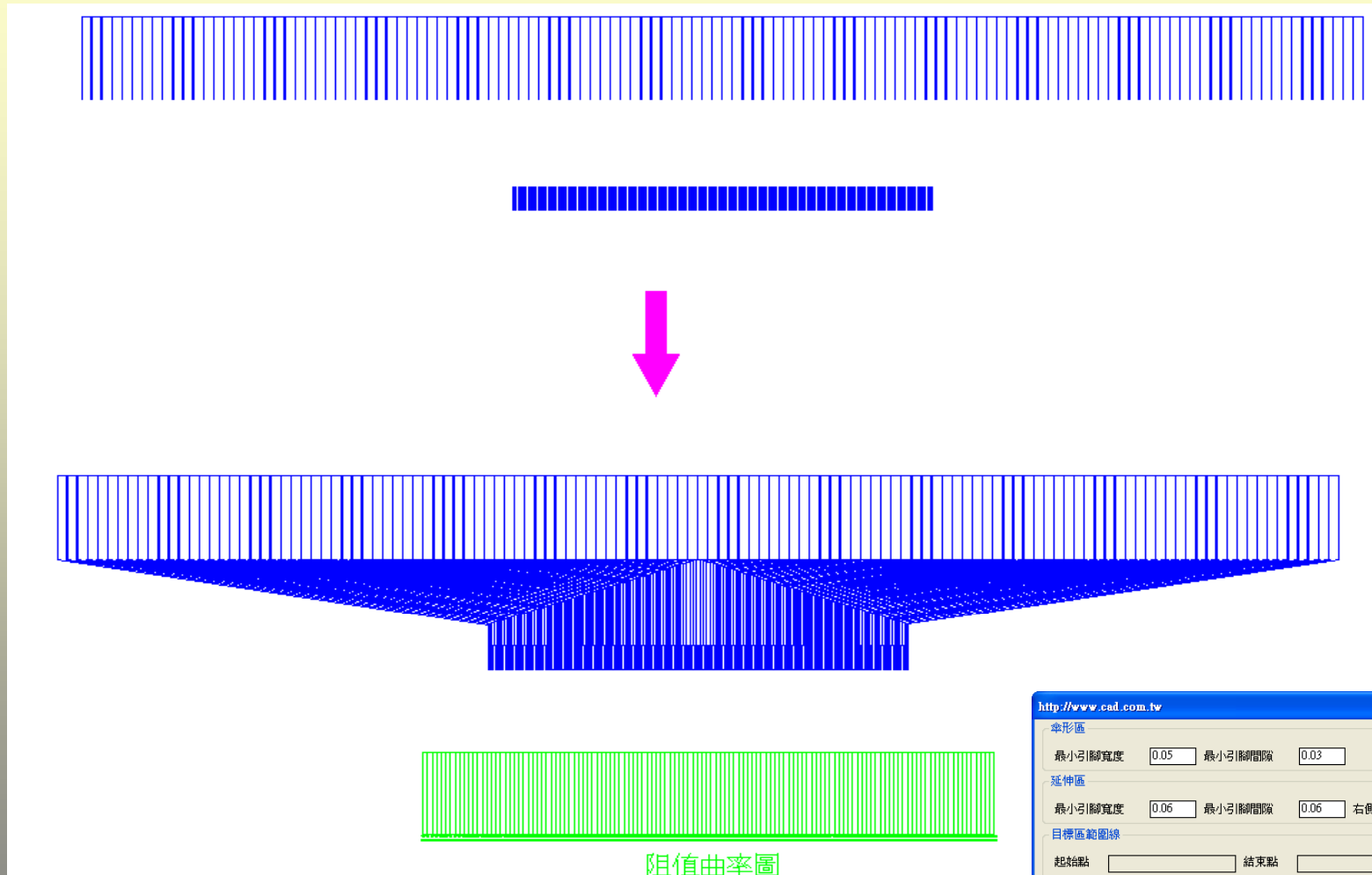
(1-1).

Common trace auto equal-“R” layout (A=B)



(2).

Electric circuit of fan equal R autolayout

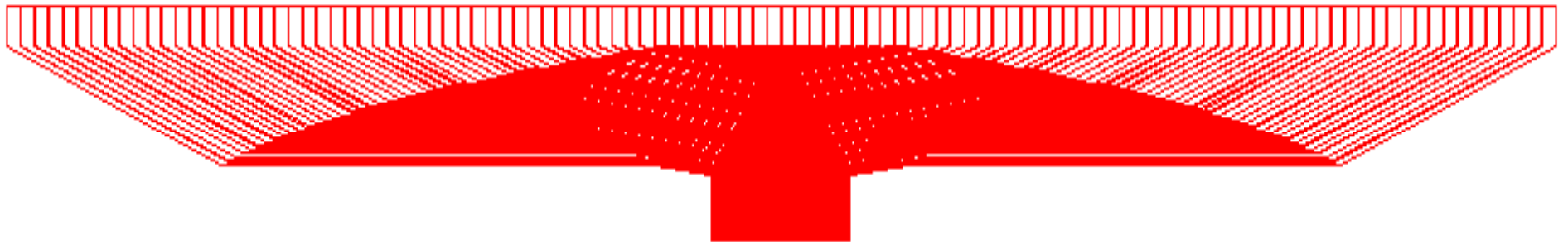


(segment area autolayout)

Segment 區直接佈局等R的接合電路



Segment and common multi application

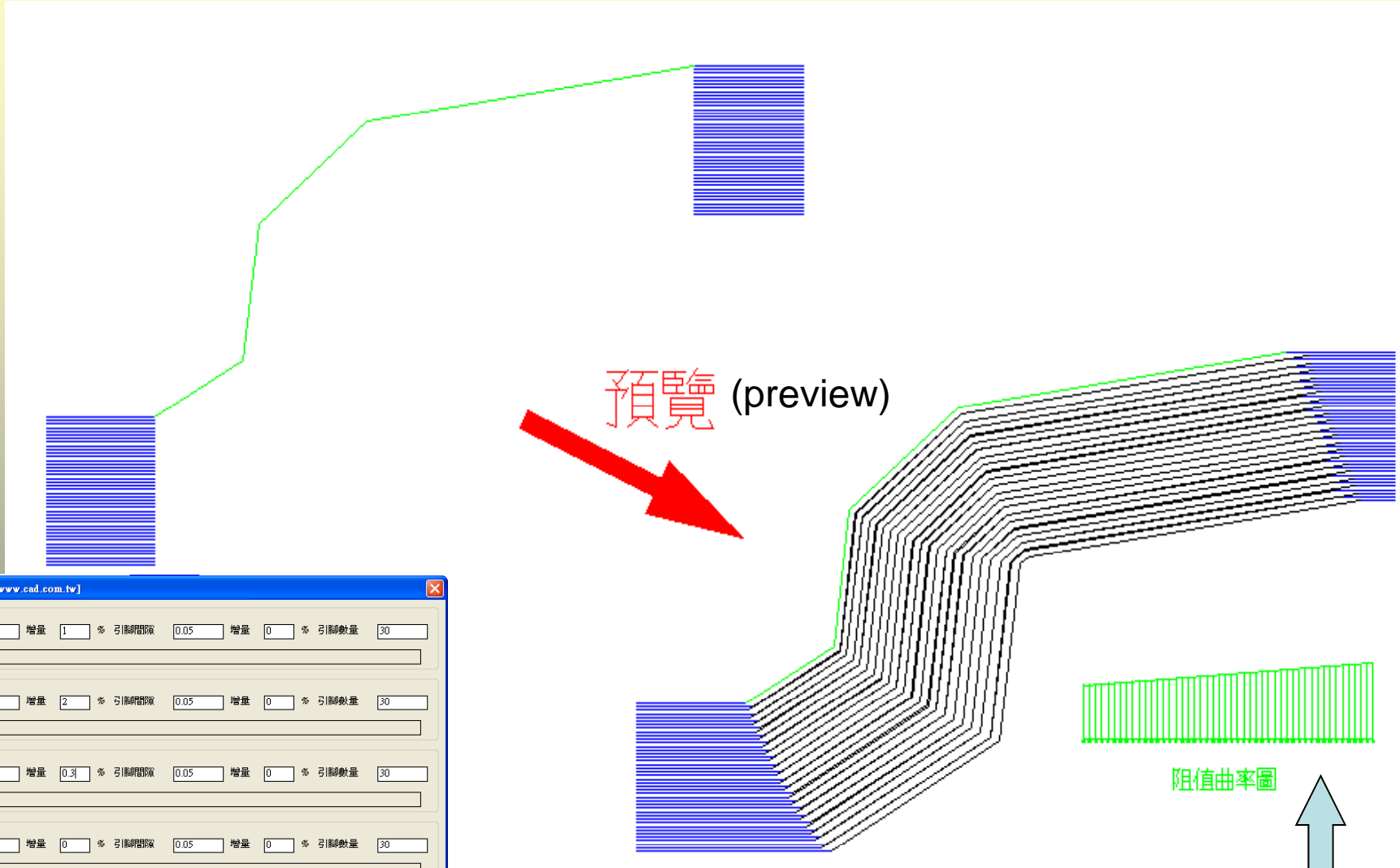


傘型擴充的等R佈局

(3).

Preview the resistance chart and final layout

可於交談框內即時調整 **width** 以利阻值均化



特殊引腳繪製 [http://www.cad.com.tw]

轉折參數一
引腳寬度 1 增量 1 % 引腳間隙 0.05 增量 0 % 引腳數量 30
 自訂間距

轉折參數二
引腳寬度 1 增量 2 % 引腳間隙 0.05 增量 0 % 引腳數量 30
 自訂間距

轉折參數三
引腳寬度 1 增量 0.3 % 引腳間隙 0.05 增量 0 % 引腳數量 30
 自訂間距

轉折參數四
引腳寬度 1 增量 0 % 引腳間隙 0.05 增量 0 % 引腳數量 30
 自訂間距

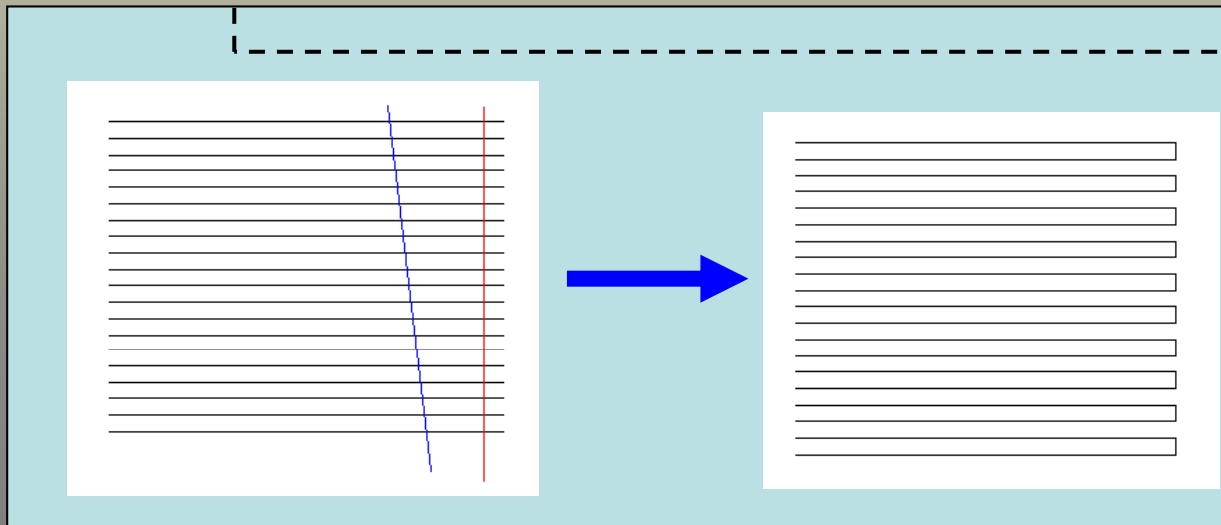
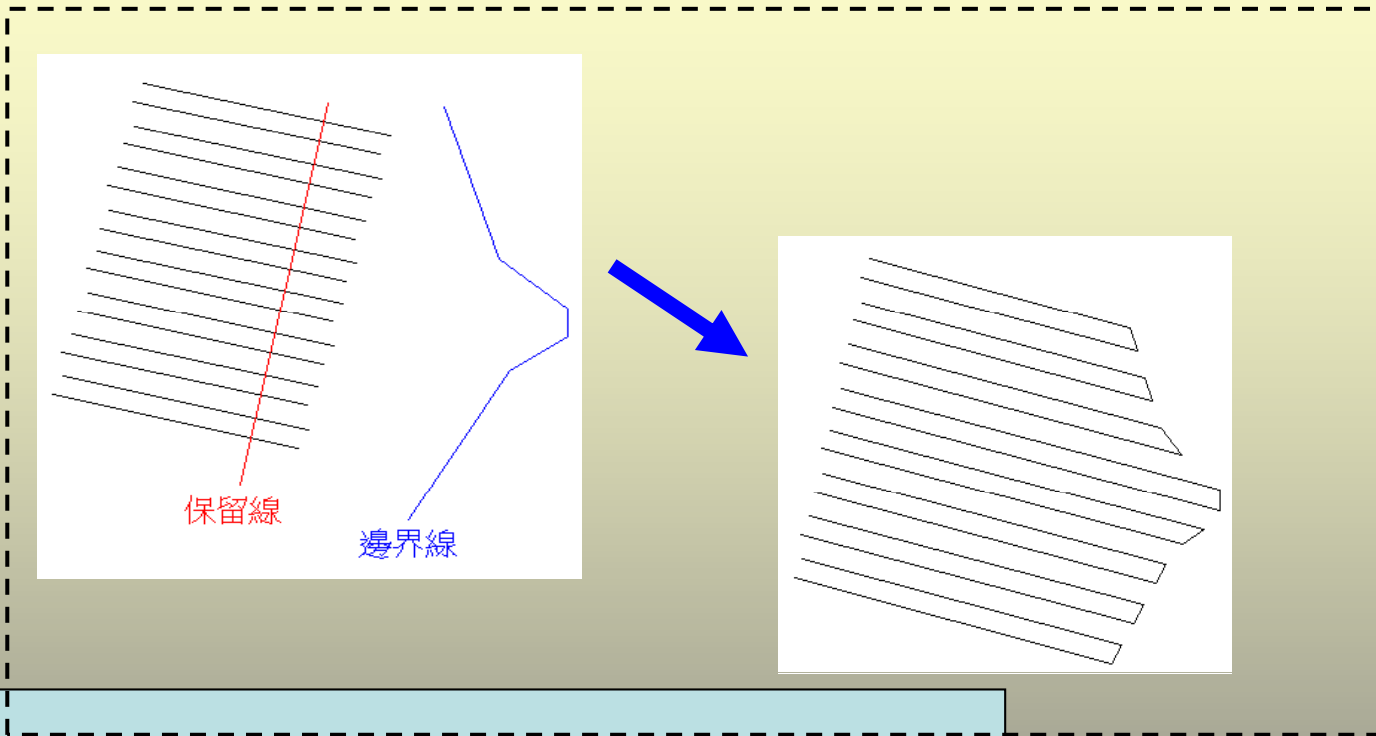
轉折參數五
引腳寬度 0.2 增量 0 % 引腳間隙 0.1 增量 0 % 引腳數量 5
 自訂間距

預視 預視R 繪製 取消

預覽接合狀況與電阻值
(resistance chart)

(4). Trace edge closed by reference line

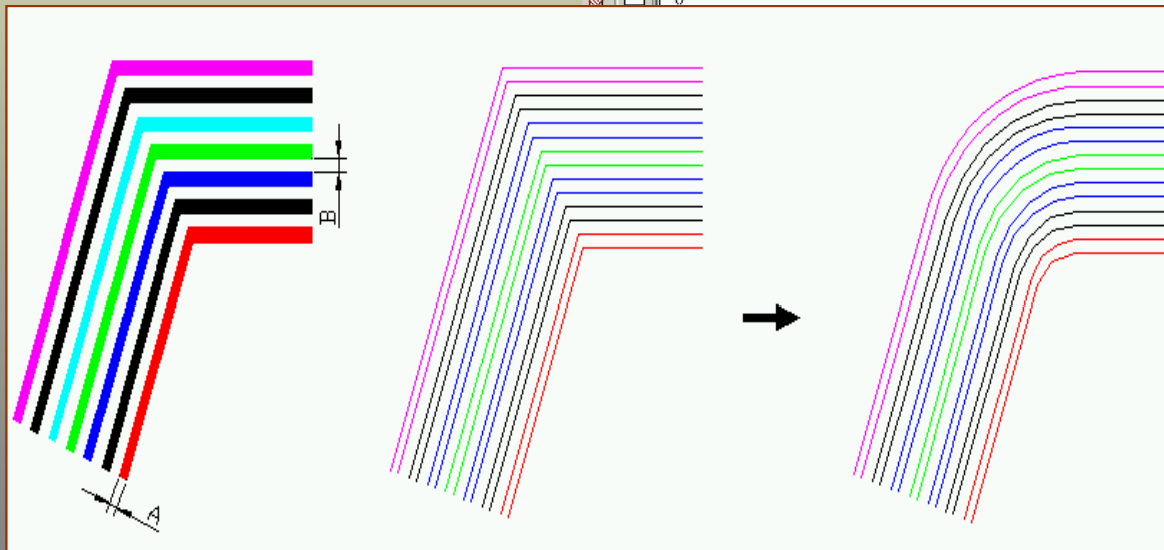
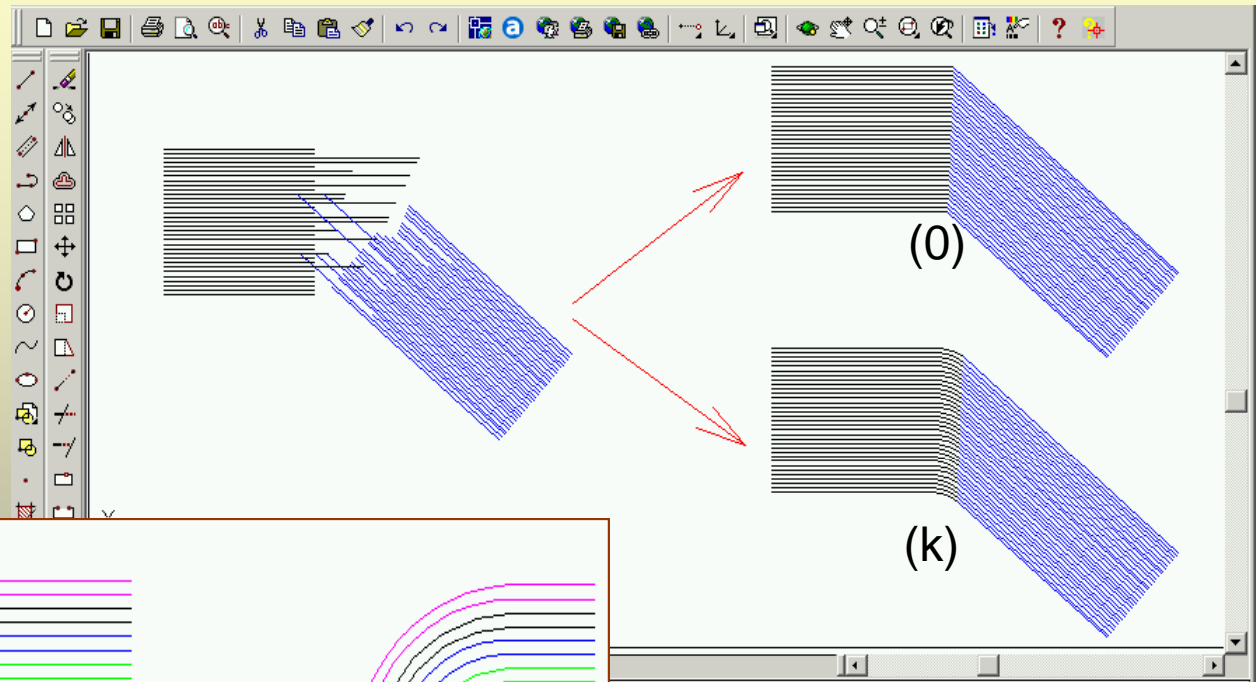
電路快速封閉延伸與修剪



(5). 兩端電路相接與快速導角作業

Auto link and fillet

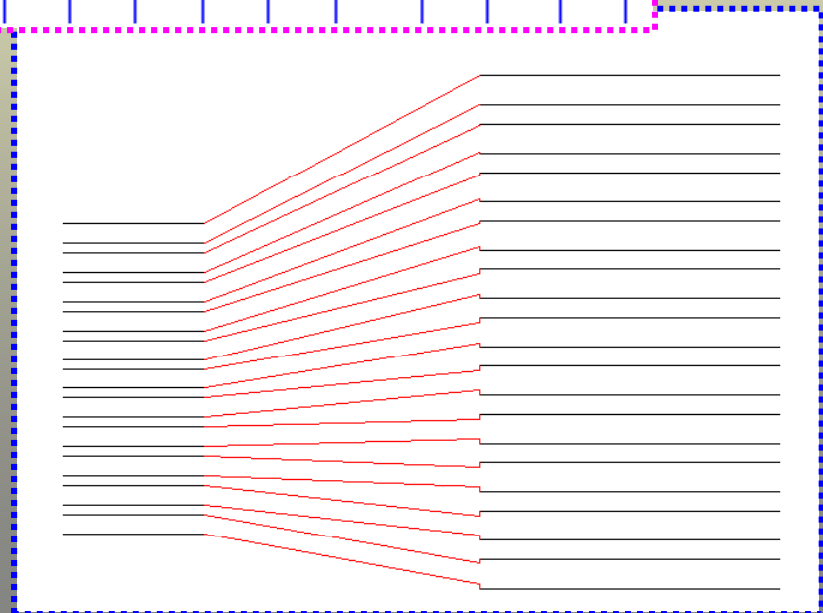
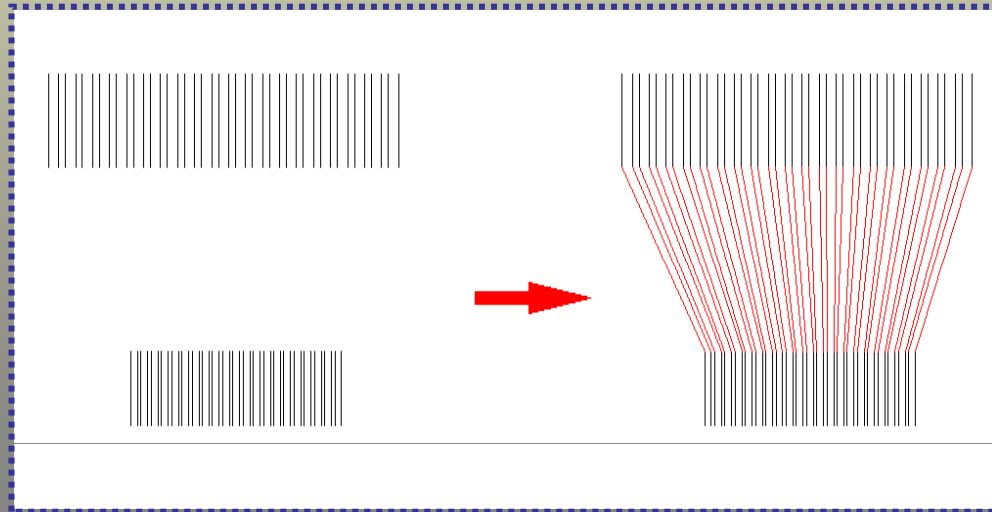
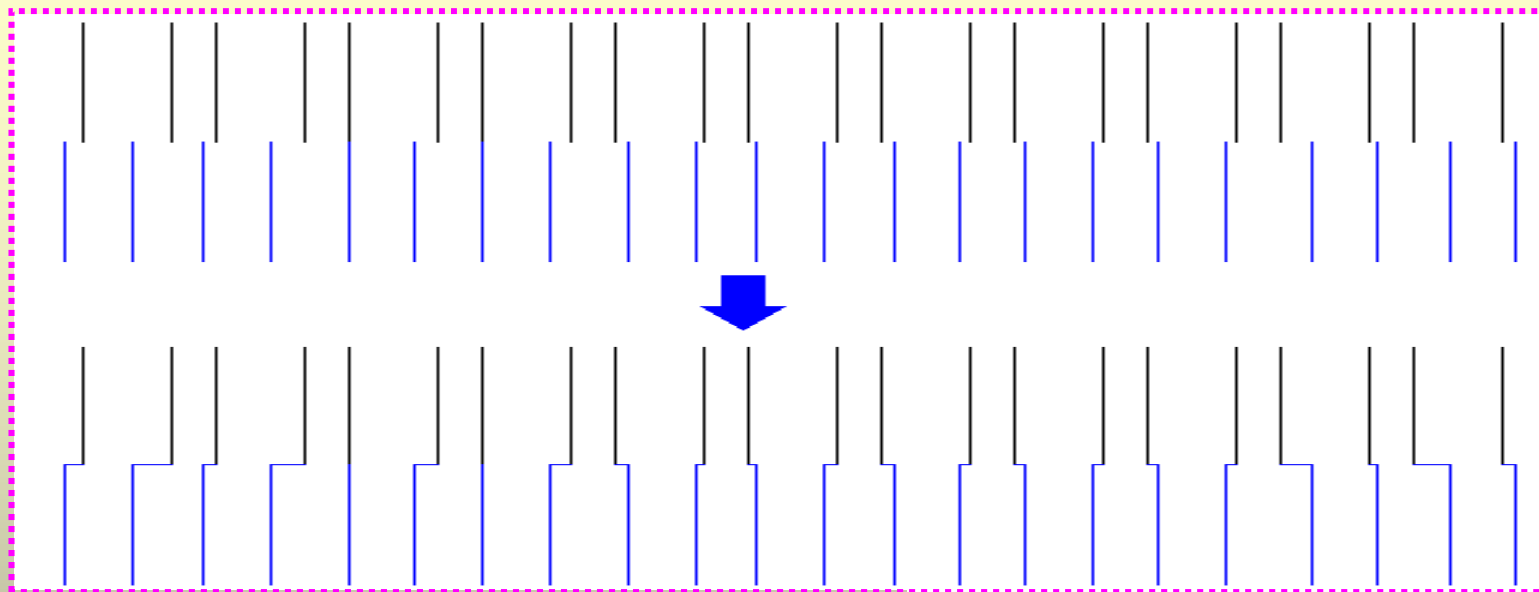
Radius = 0 V.S Radius = K



變化 R 應用 (Variety radius)

(6).

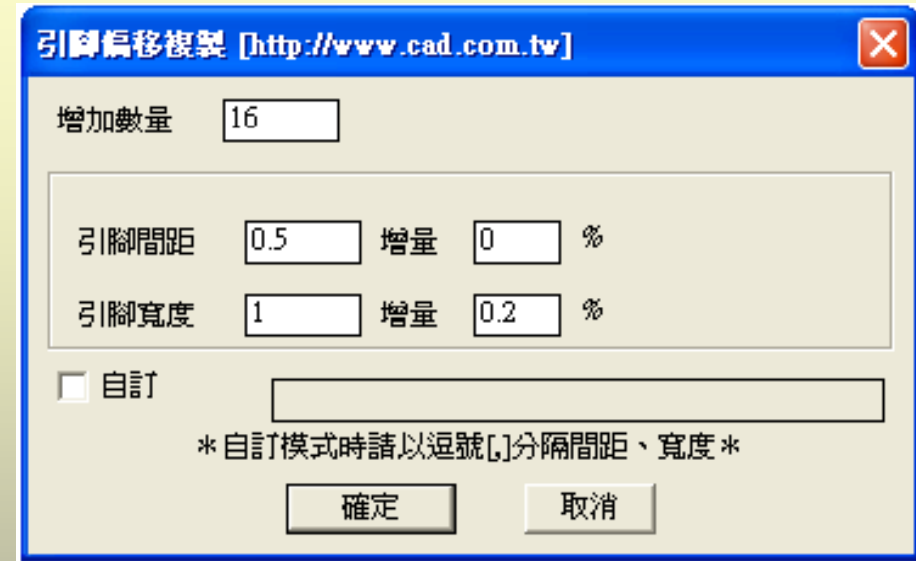
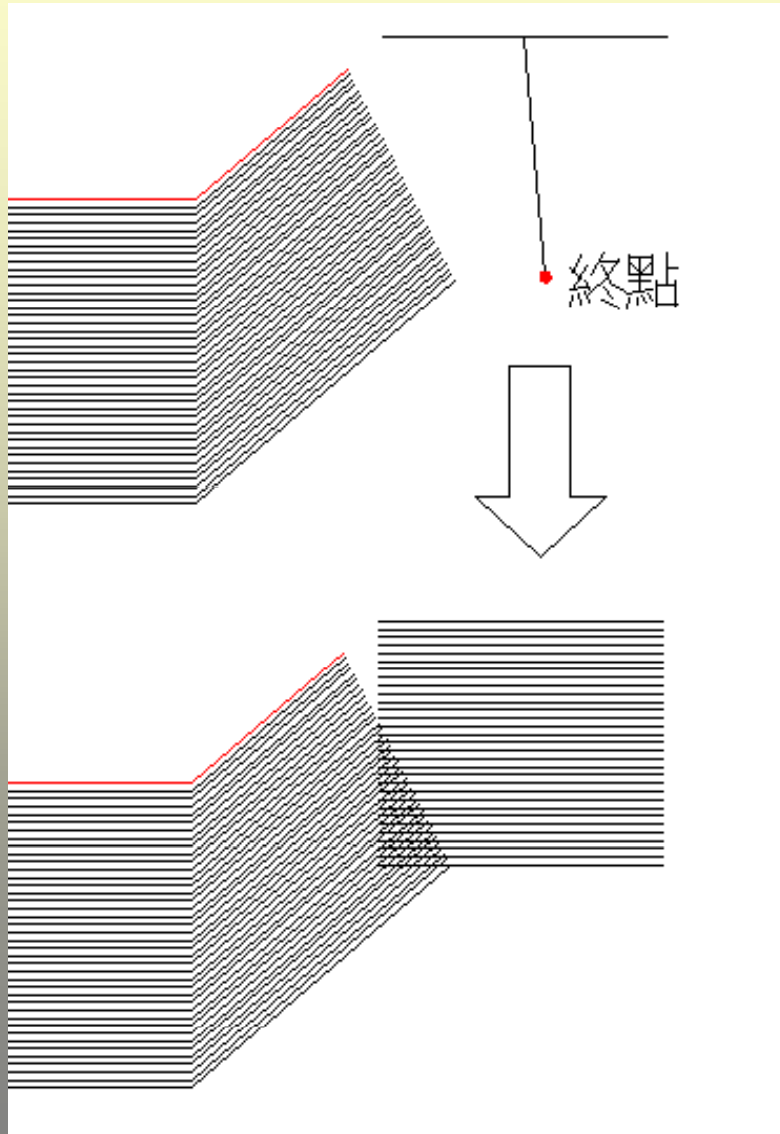
Auto link of Trace end-point



(equal R of link)

(7).

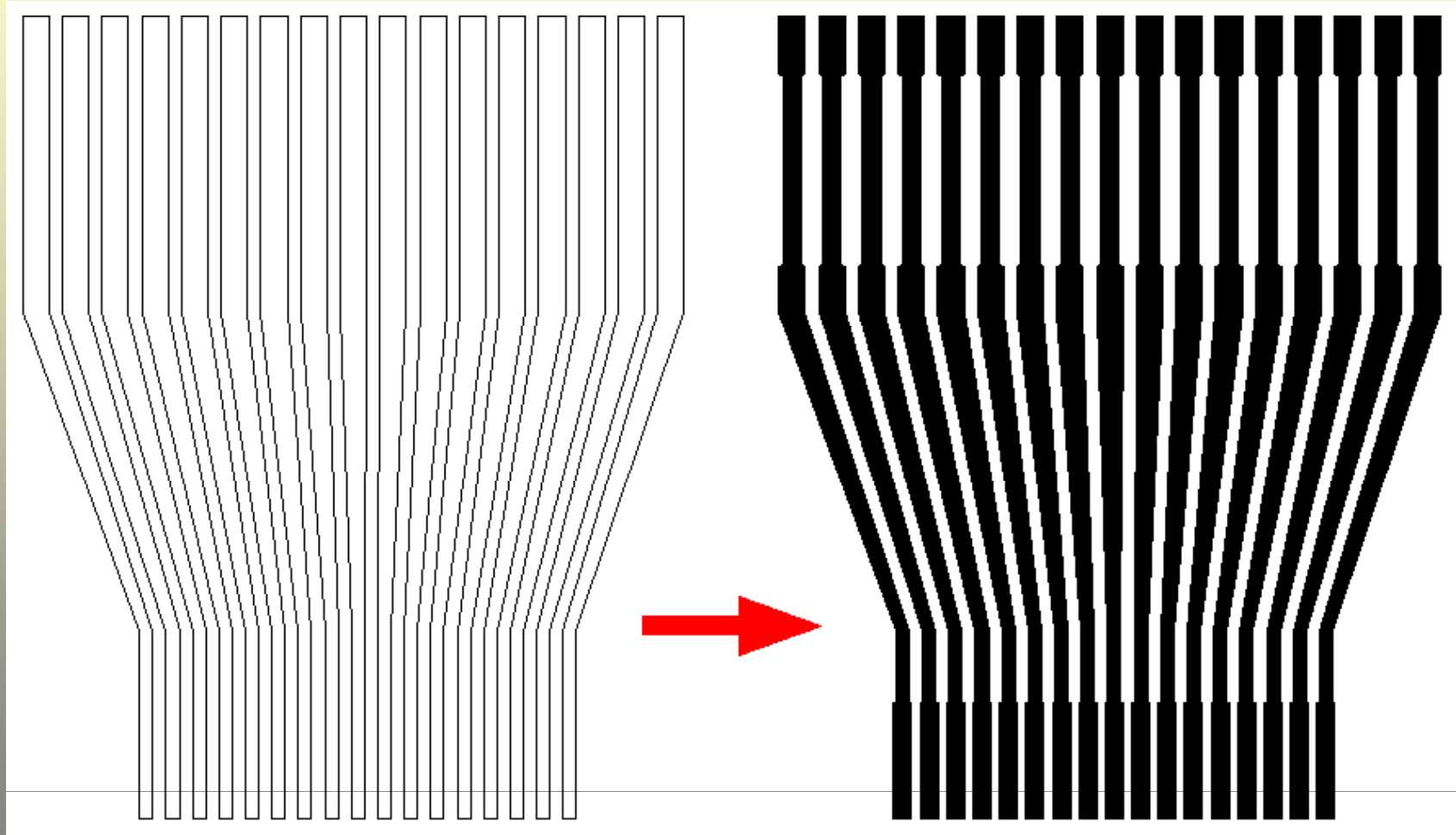
Trace offset and copy



1. 偏移複製不限方向 (offset to any direction)
2. Increase quantity of width & space

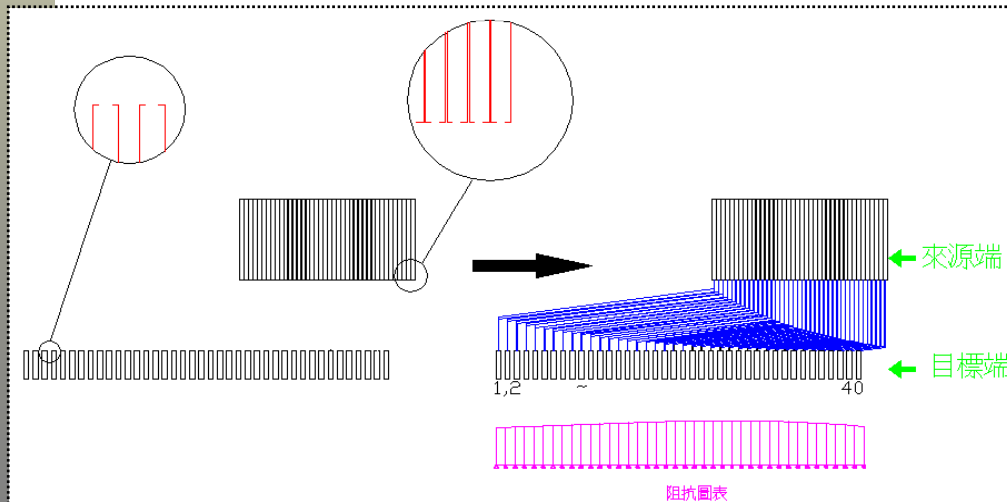
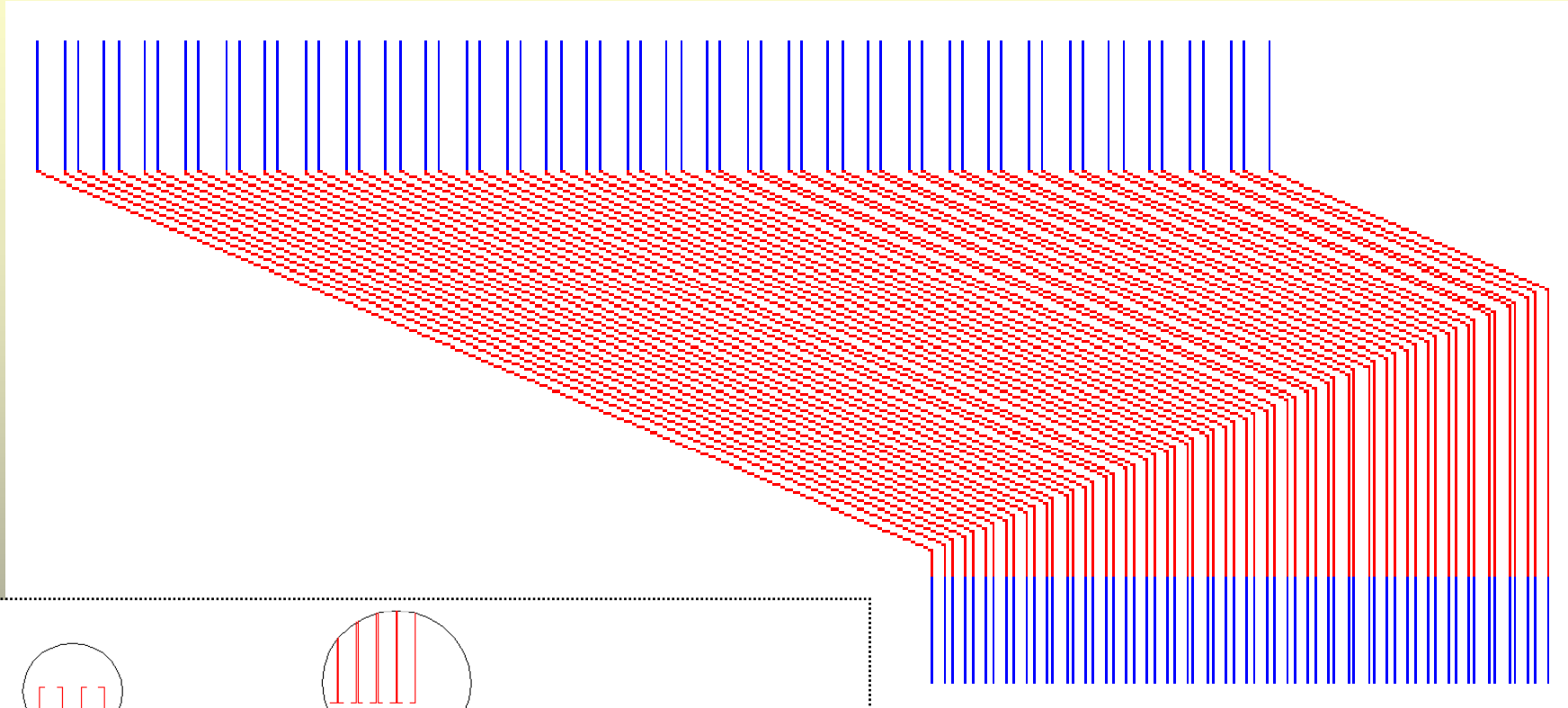
(8).

批次改變電路的局部寬度
(Change width of trace part)



(9).

電路延伸轉折連接



自動產生紅色接線

(Generation red line for link)

(10).

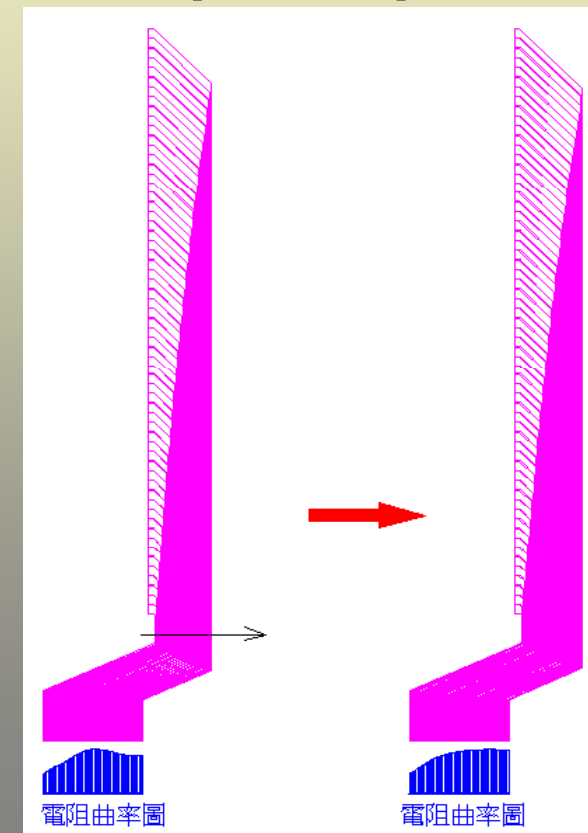
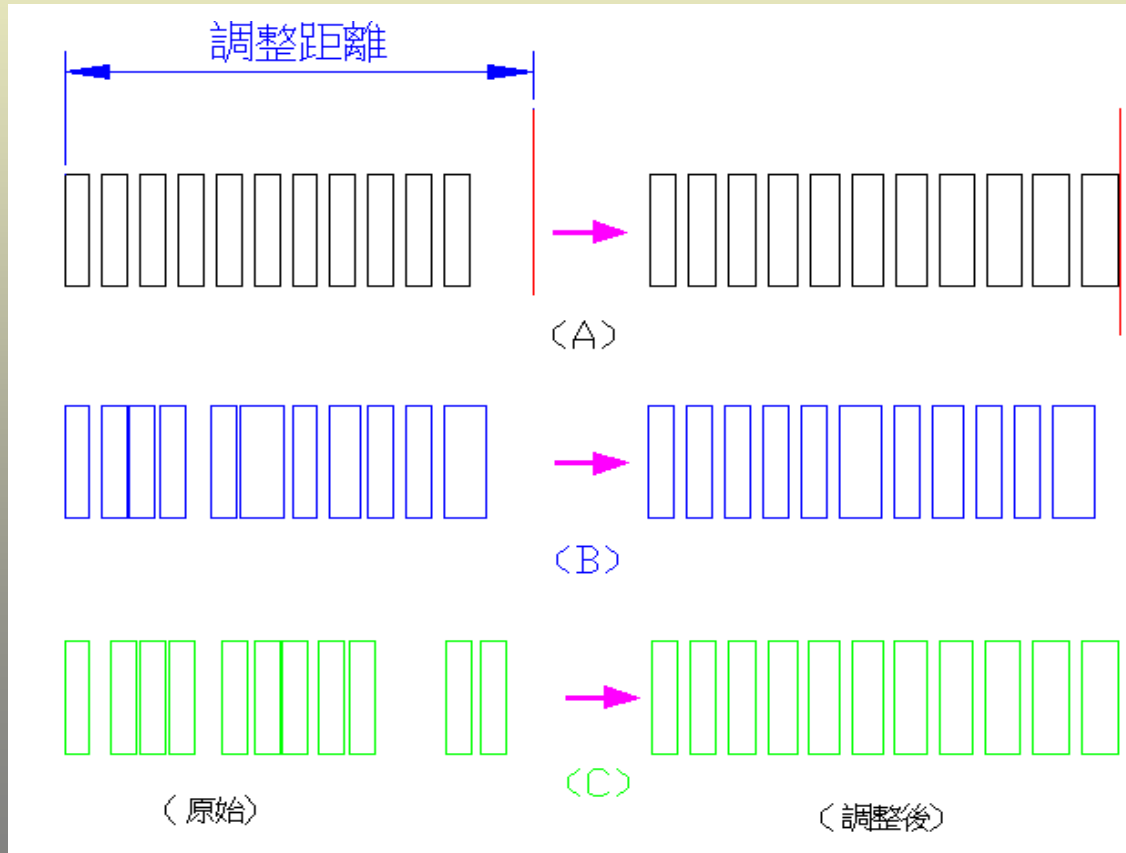
Width & Space adjustment

(快速調整阻值均化作業)

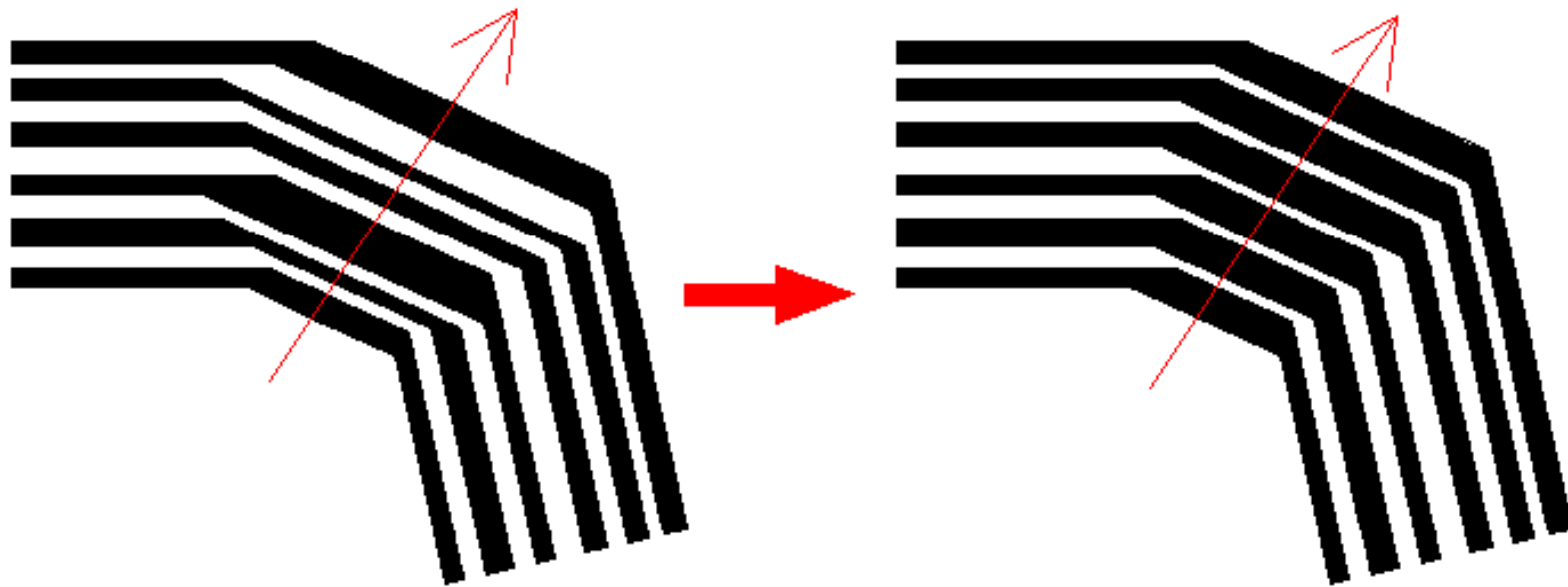
- 1-1. +- 寬度值(for width)
- 1-2. 等差遞增/遞減
- 1-3. 等比遞增/遞減
- 1-4. 重新定義 min width & min space

Width 為漸進式的遞增/減
Space 保持在 min-space

[調整案例]



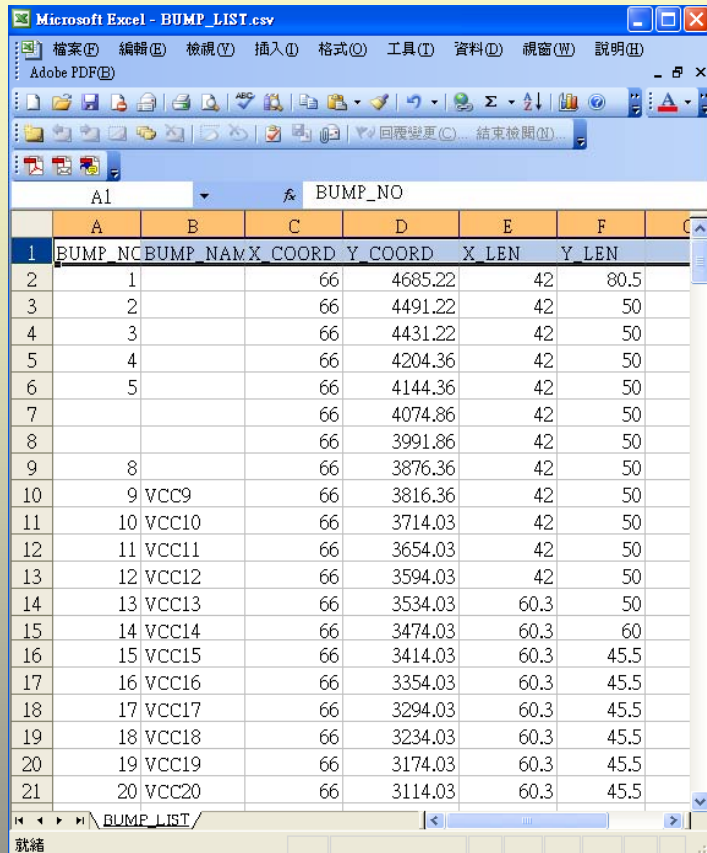
(10-1). trace width & space adjustment



將平行區段的電路重新安排 width 與 space

(11).

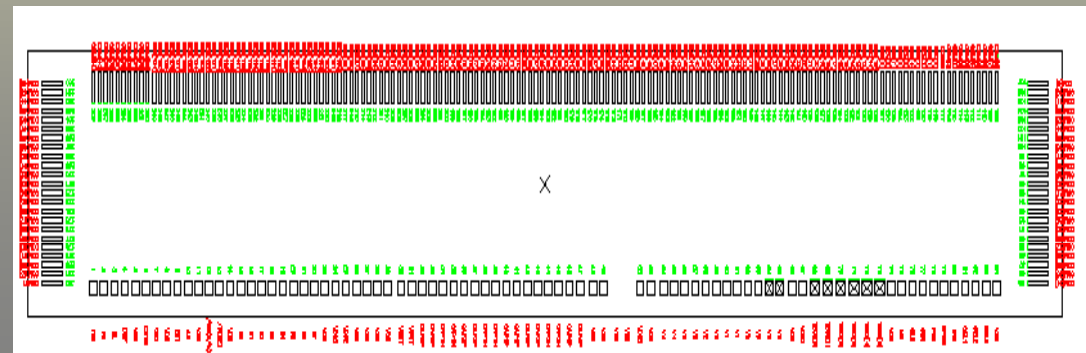
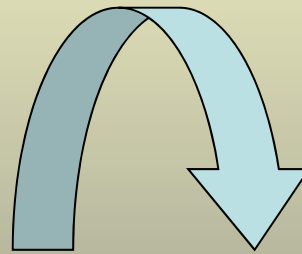
Drawing Chip and bump by Coordinates file



Microsoft Excel - BUMP_LIST.csv

	A	B	C	D	E	F
1	BUMP_NO	BUMP_NAME	X_COORD	Y_COORD	X_LEN	Y_LEN
2	1		66	4685.22	42	80.5
3	2		66	4491.22	42	50
4	3		66	4431.22	42	50
5	4		66	4204.36	42	50
6	5		66	4144.36	42	50
7			66	4074.86	42	50
8			66	3991.86	42	50
9	8		66	3876.36	42	50
10	9	VCC9	66	3816.36	42	50
11	10	VCC10	66	3714.03	42	50
12	11	VCC11	66	3654.03	42	50
13	12	VCC12	66	3594.03	42	50
14	13	VCC13	66	3534.03	60.3	50
15	14	VCC14	66	3474.03	60.3	60
16	15	VCC15	66	3414.03	60.3	45.5
17	16	VCC16	66	3354.03	60.3	45.5
18	17	VCC17	66	3294.03	60.3	45.5
19	18	VCC18	66	3234.03	60.3	45.5
20	19	VCC19	66	3174.03	60.3	45.5
21	20	VCC20	66	3114.03	60.3	45.5

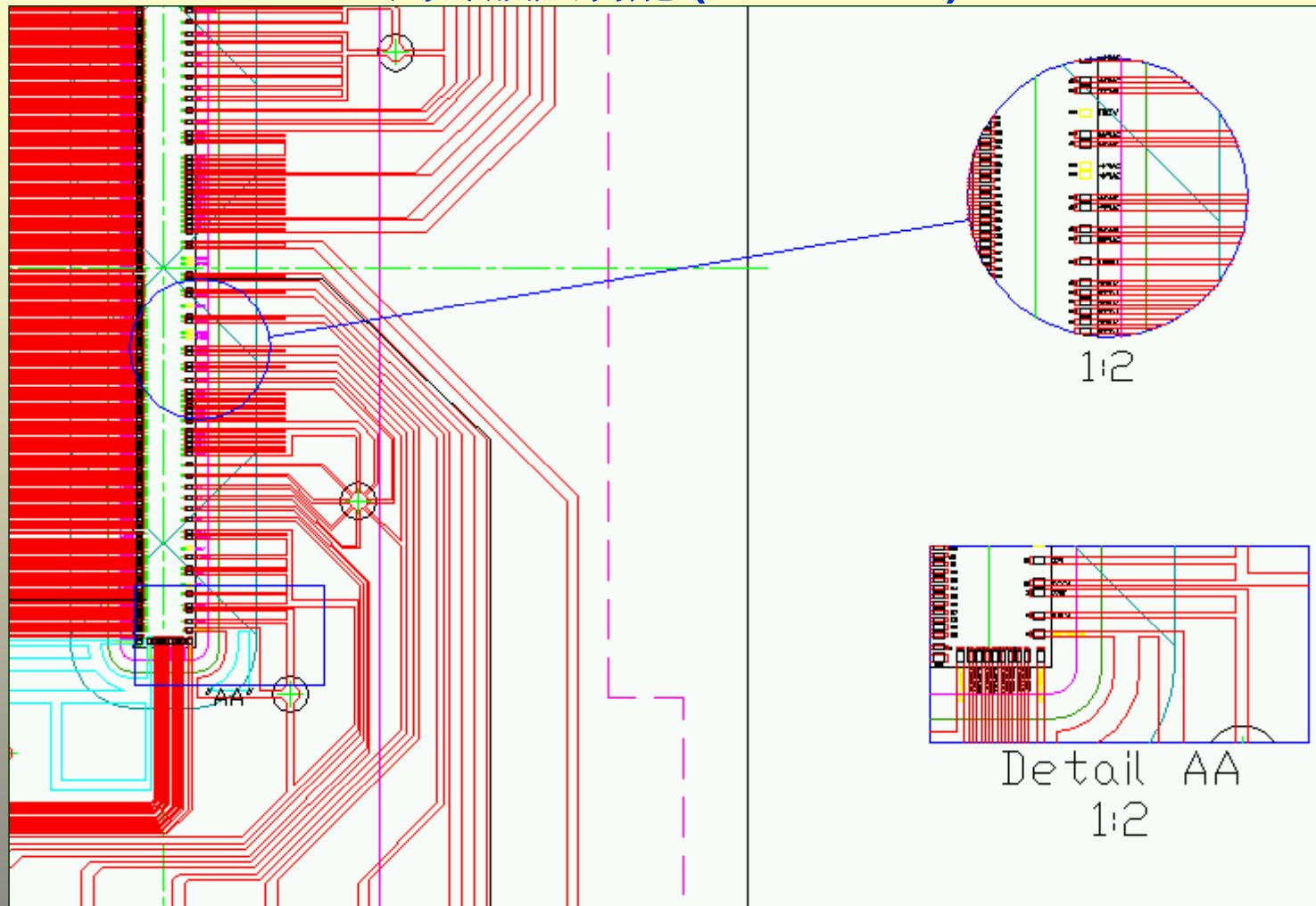
依座標檔自動繪出 chip/bump
bump no. / bump netname



(12).

Darwing detail view by define area

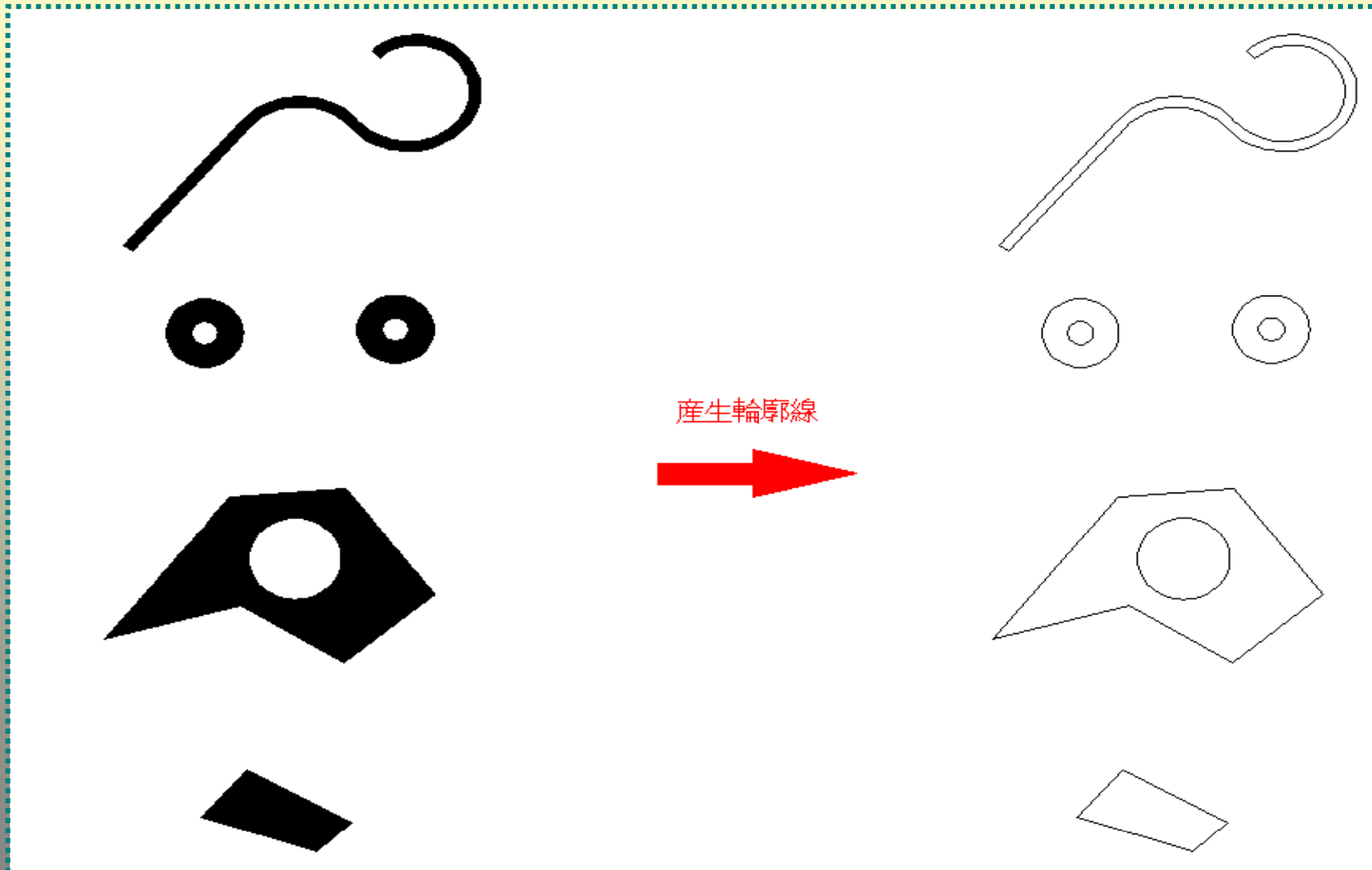
局部放大功能 (detail view)



放大範圍可為圓形與矩形

(13).

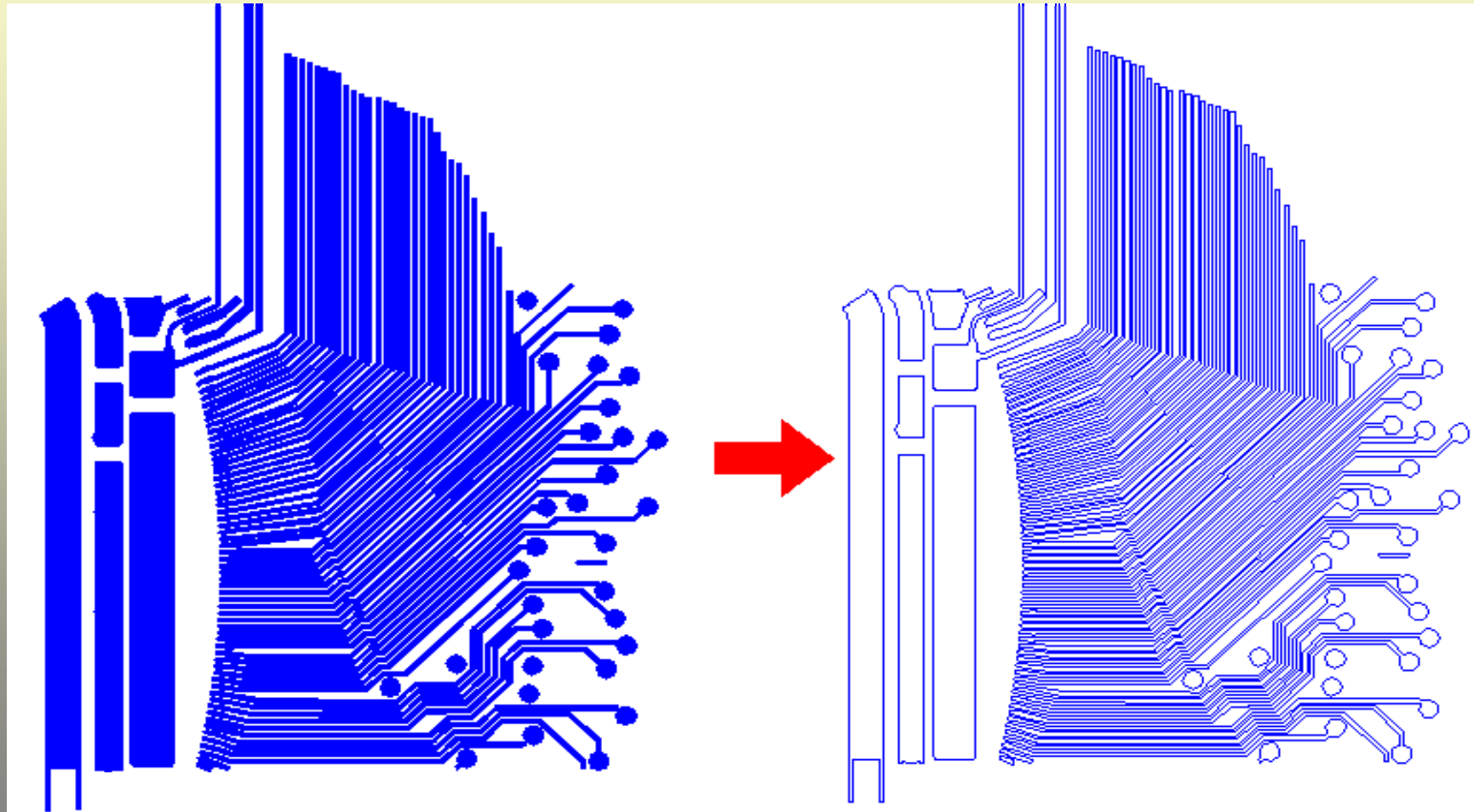
Generation object outline



(pline,solid,donut,hatch)

(13-1).

Auto generation electric circuit outline line



(14).

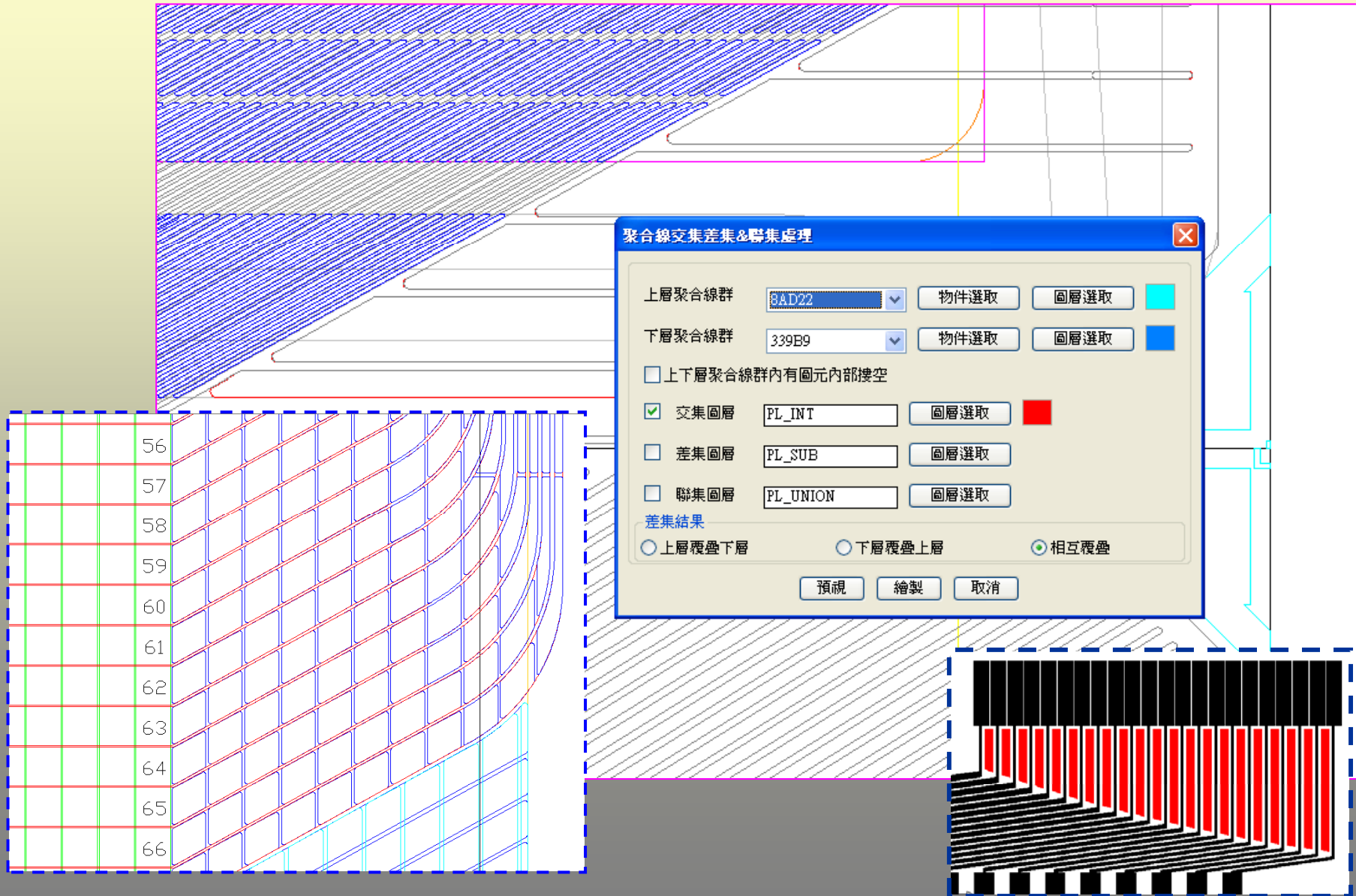
The text consecution serial number and attribute modify

The diagram illustrates the process of modifying text consecution serial numbers and attributes. It consists of three main parts:

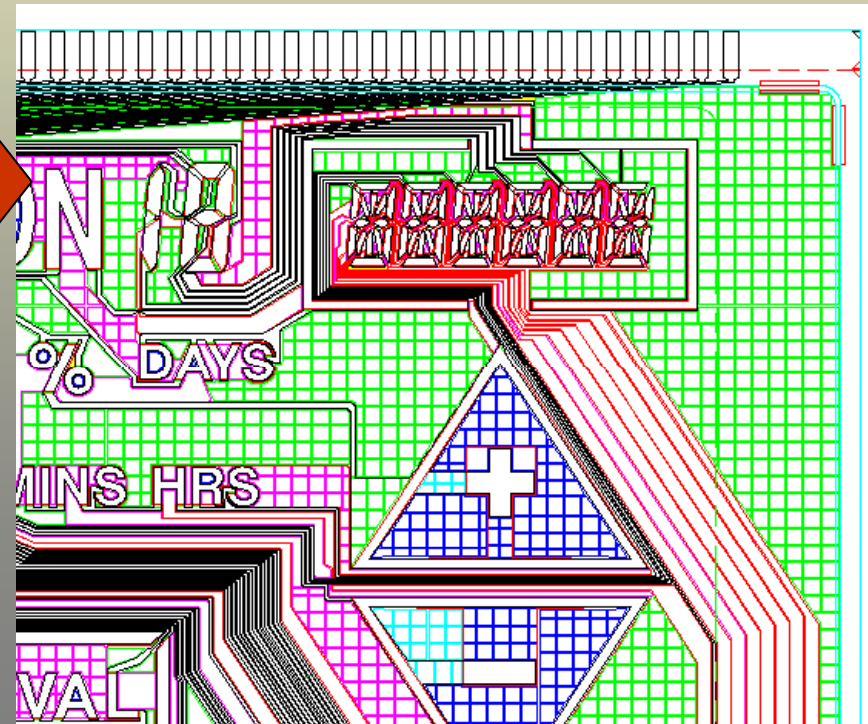
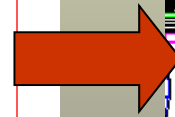
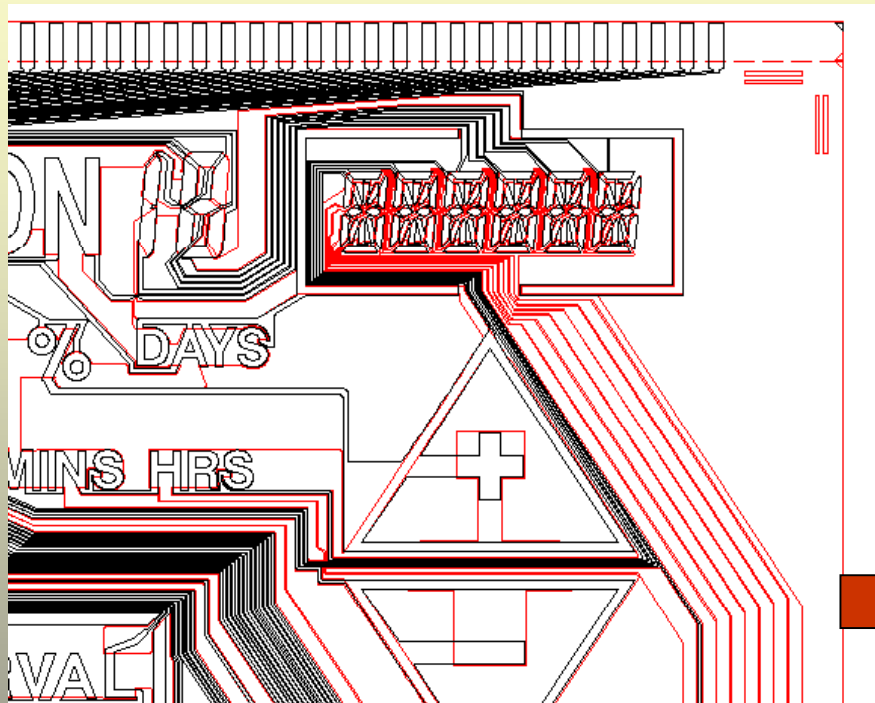
- Top Left:** A sequence of 16 empty rectangular text boxes, numbered 1 through 16 above them.
- Top Right:** A dialog box titled "改變文字屬性 [http://www.cad.com.tw]". It contains the following fields:
 - 前置字串 (Prefix string): SEG(
 - 後置字串 (Suffix string):)
 - 文字字高 (Text height):
 - 文字角度 (Text angle): 90
 - 縮放比例 (Scale factor): 1.2
 - 文字圖層 (Text layer):Buttons for "確定" (OK) and "取消" (Cancel) are at the bottom.
- Bottom:** A sequence of 16 segmented text boxes, labeled SEG(1) through SEG(16) above them. A red arrow points from the first box to the 10th box, which contains the number 10. The 11th box contains 11, the 12th contains 12, the 13th contains 13, the 14th contains 14, the 15th contains 15, and the 16th contains 17. A blue curved arrow points from the top-left sequence of boxes to the segmented boxes.

(15).

Dummy trace design automatically

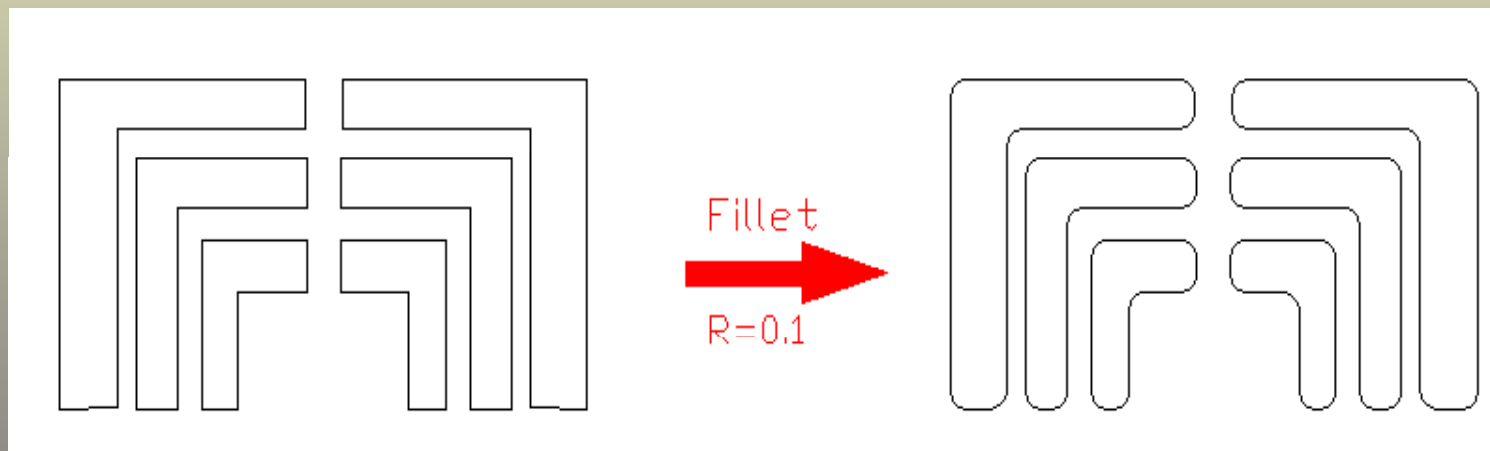
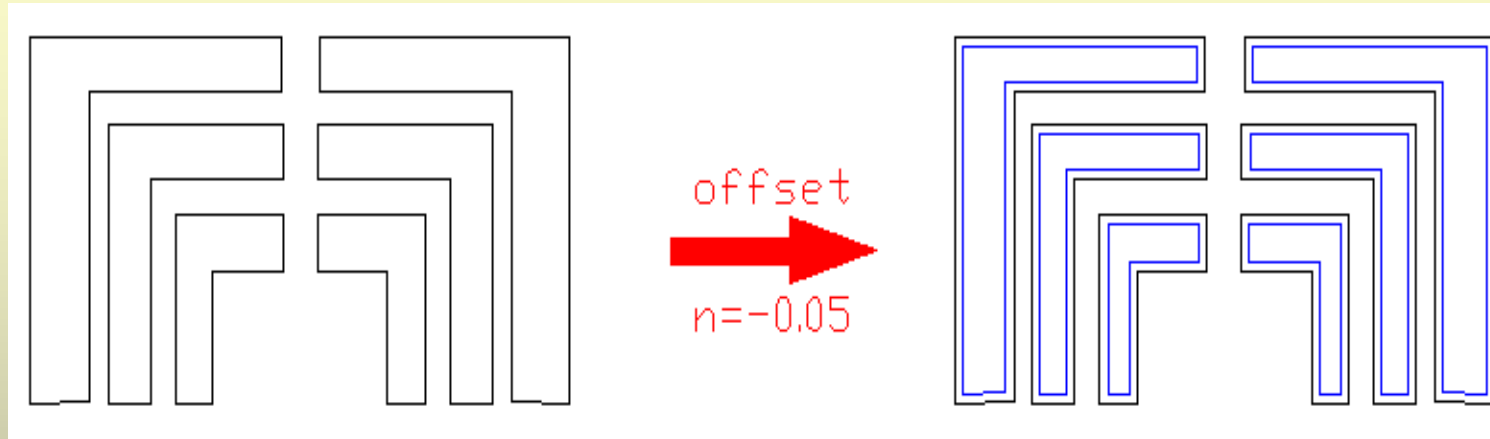


Auto draw to repair box dummy



(15).

The whole offset and fillet

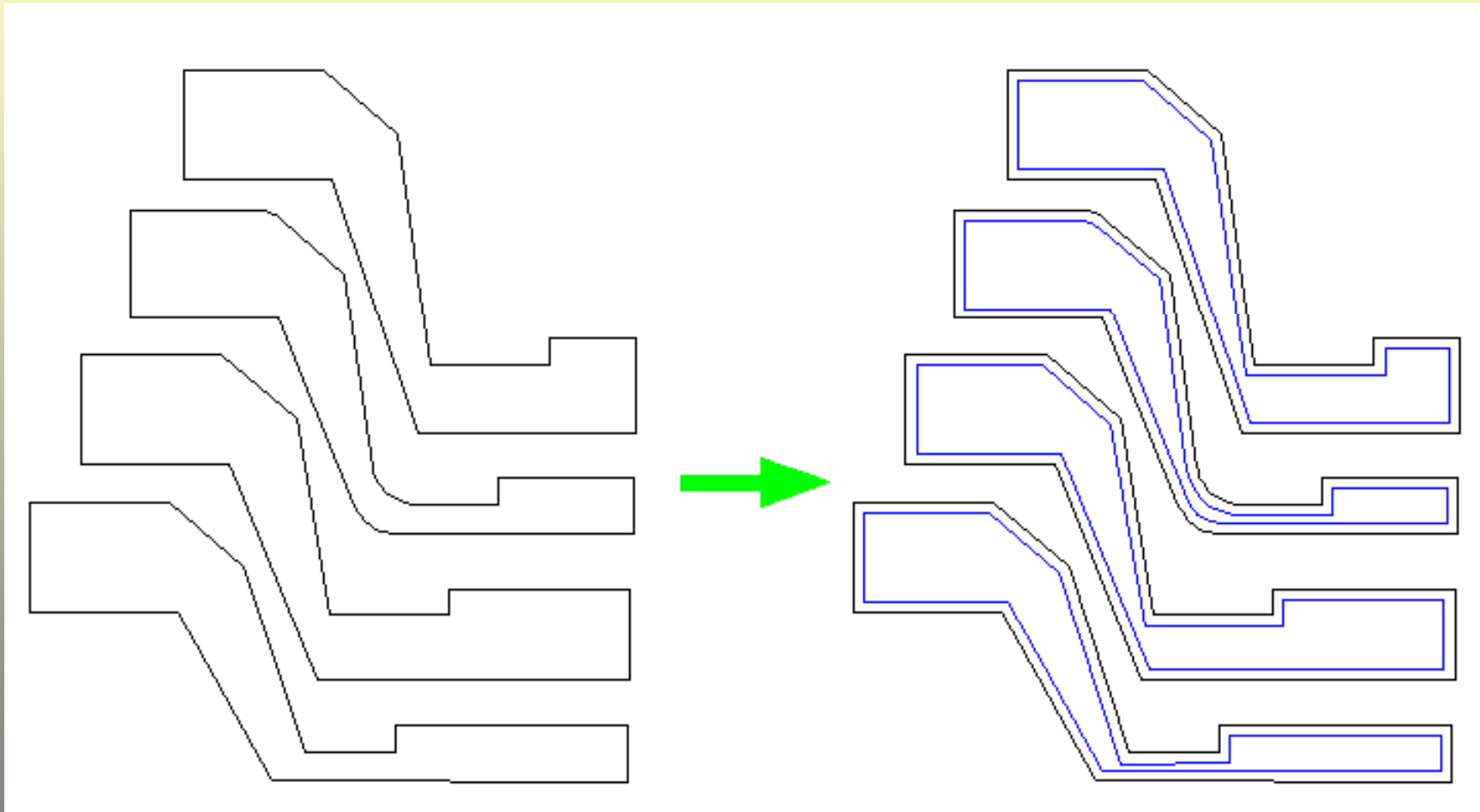


(After canning choose much a processing)

(15-1).

Close pline whole do offset

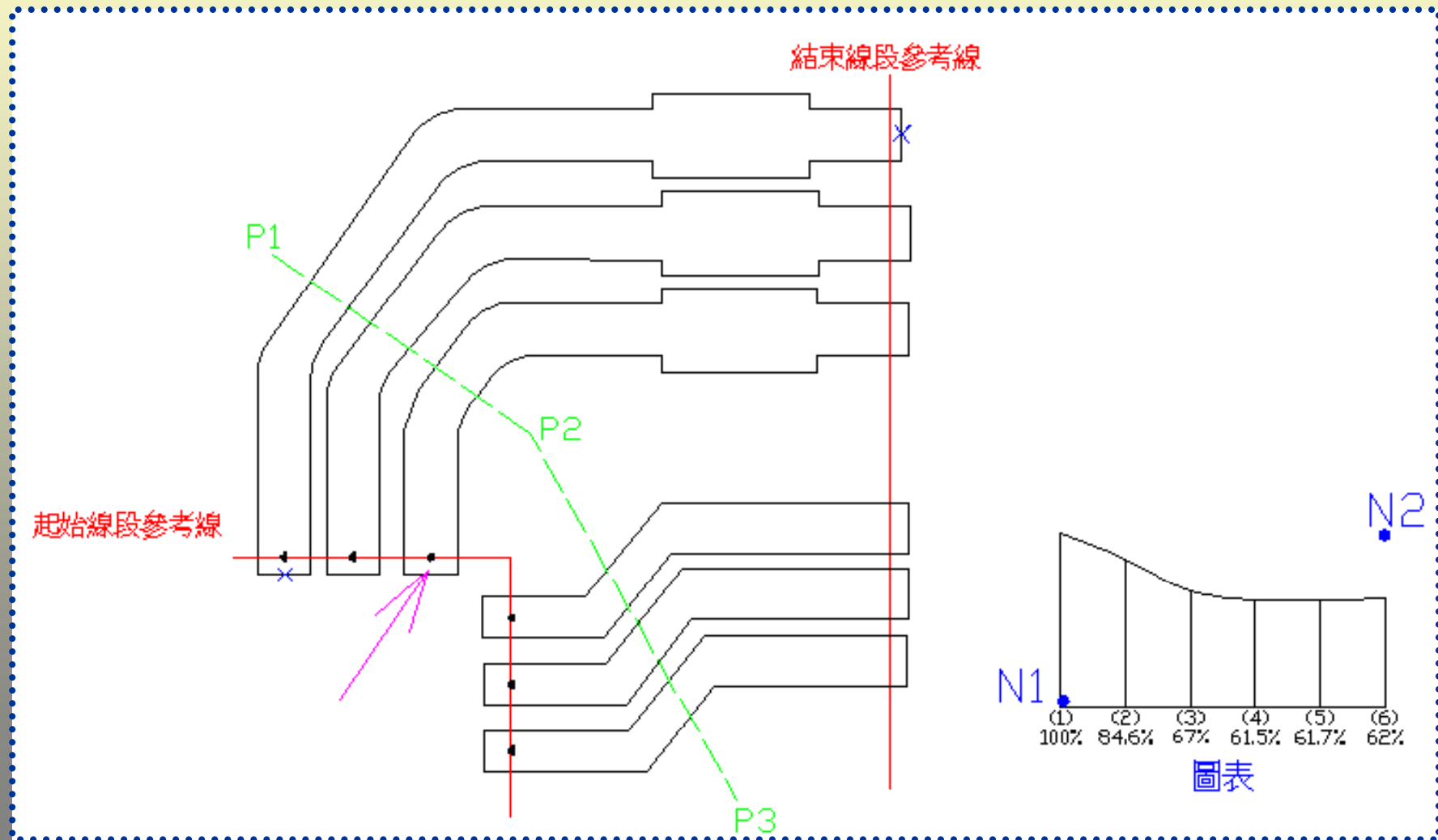
(Can go toward outside or go toward inside)



(貳)

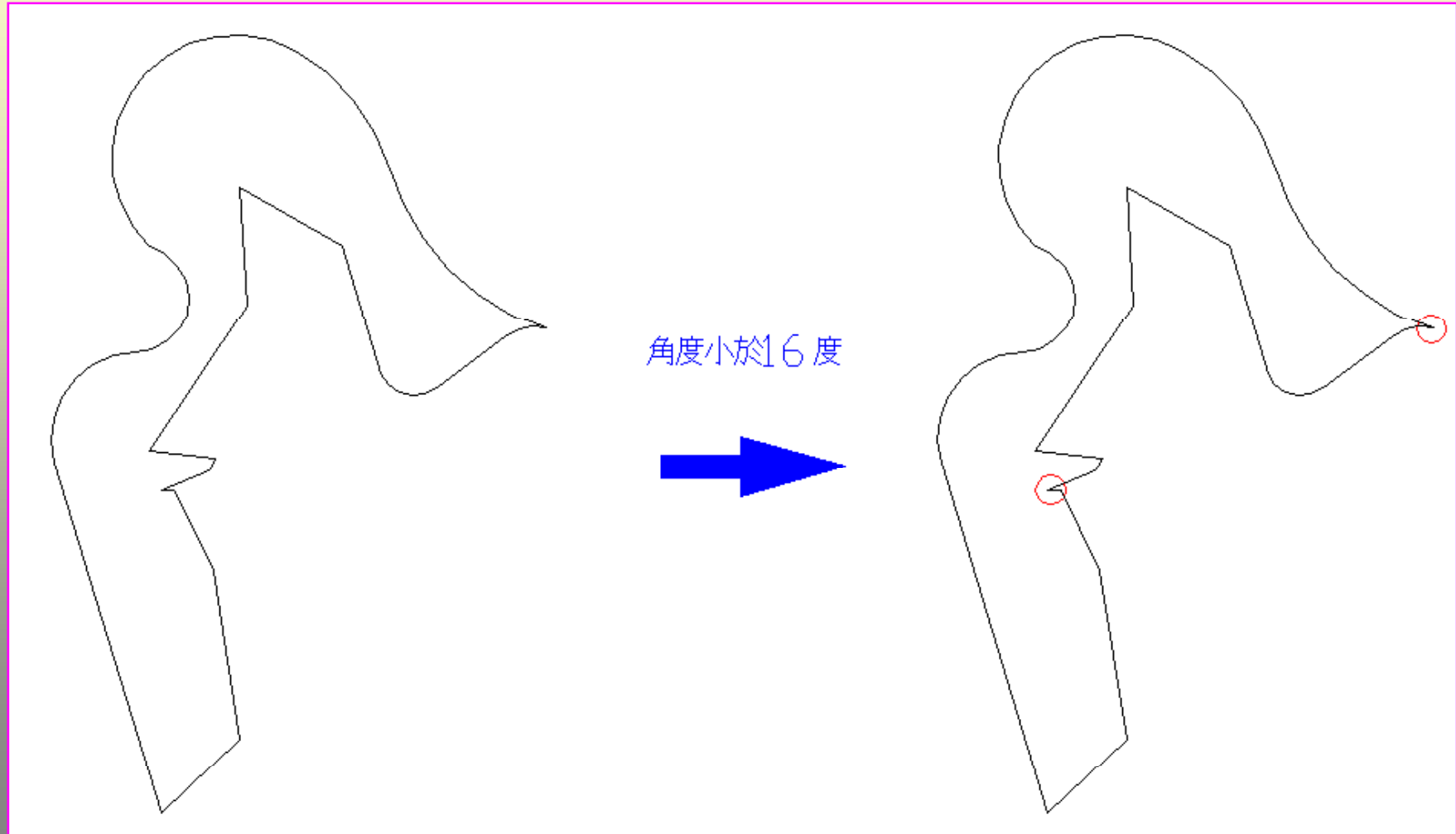
LCD ITO trace checking and Analysis

(1). Resistance analysis :



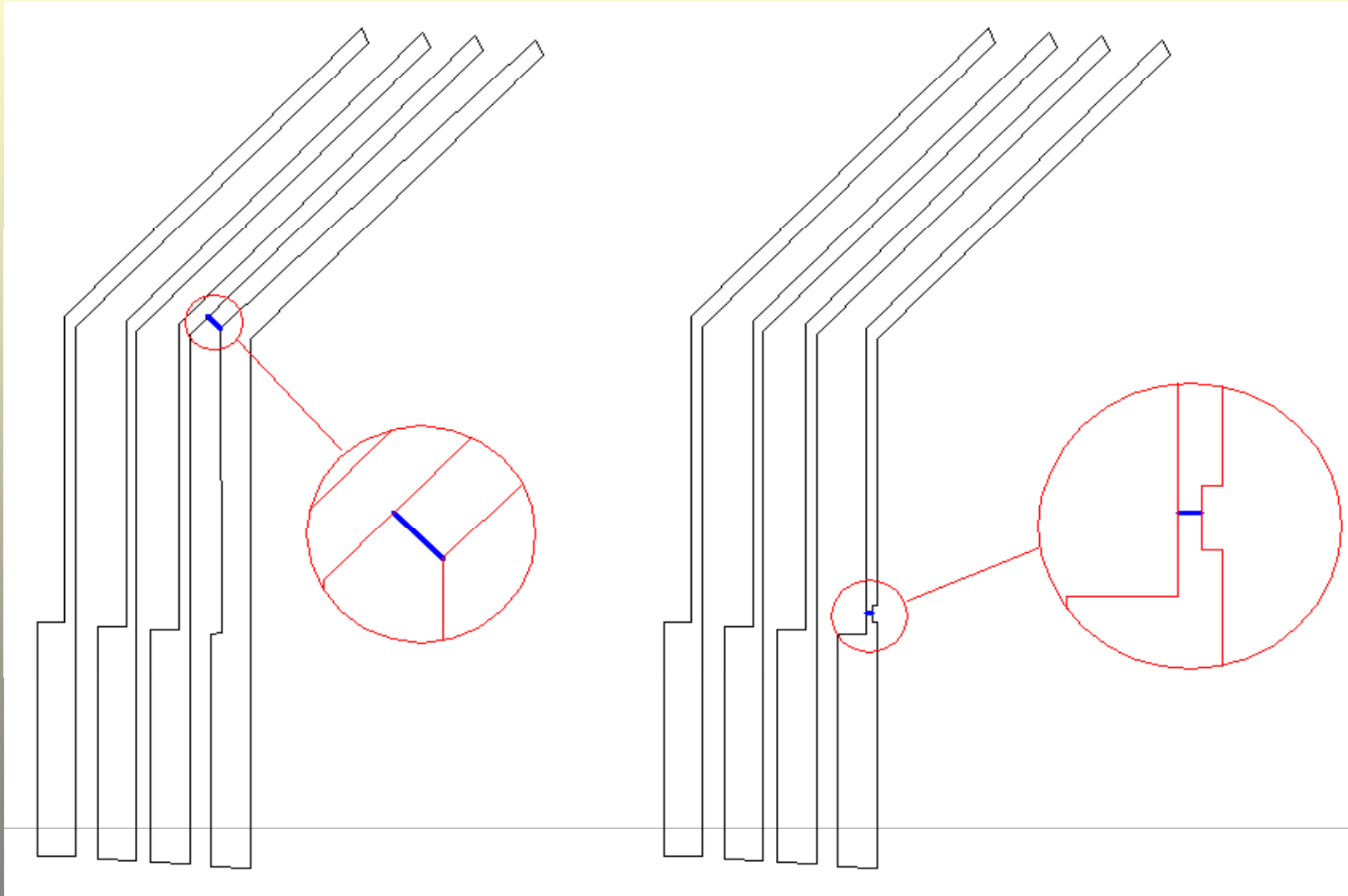
(2).

**Check the turning of the electric circuit
absurdity corn, examine for the convenience
of the quality of the electric circuit**



(3).

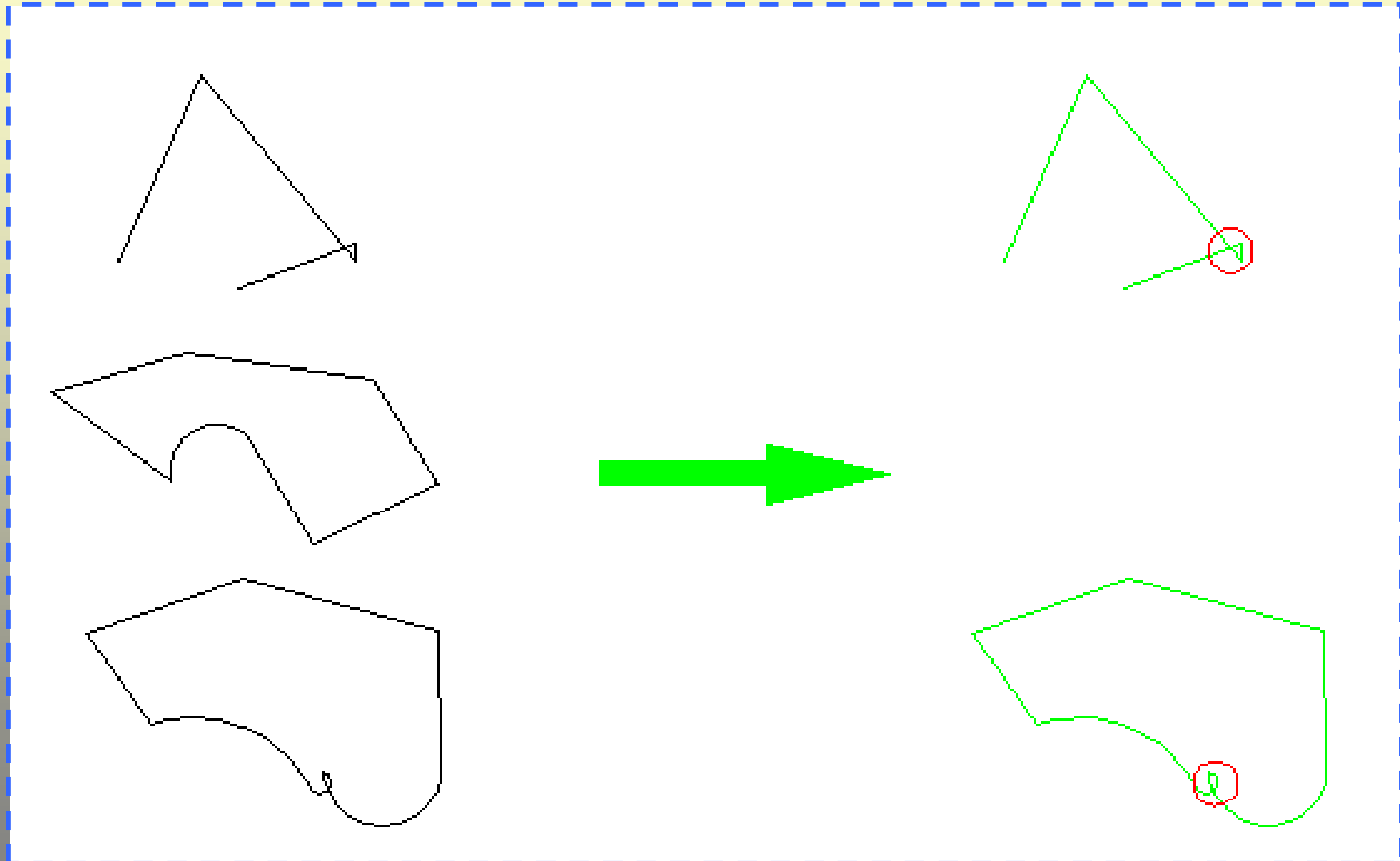
自動檢查 min width 與 min space



(min space checking)

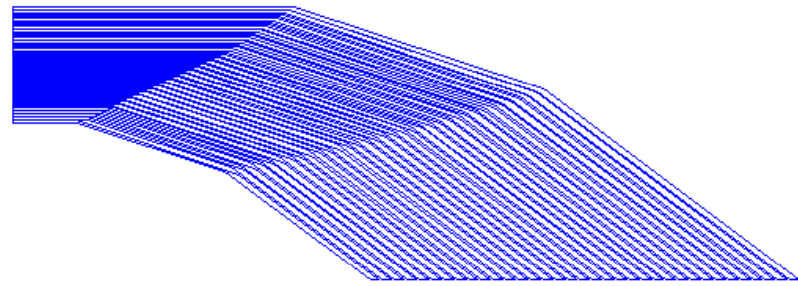
(min width checking)

(4). **Checking crossing trace(closed pline)**

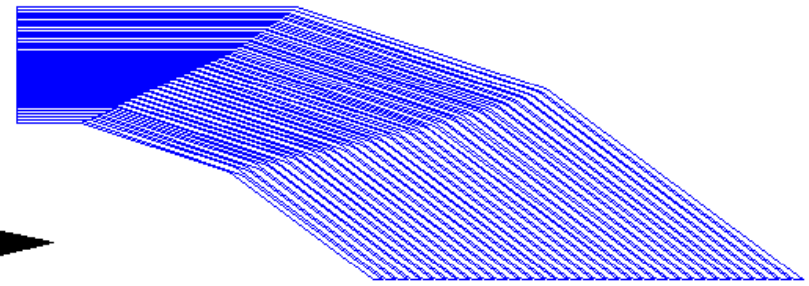


(5).

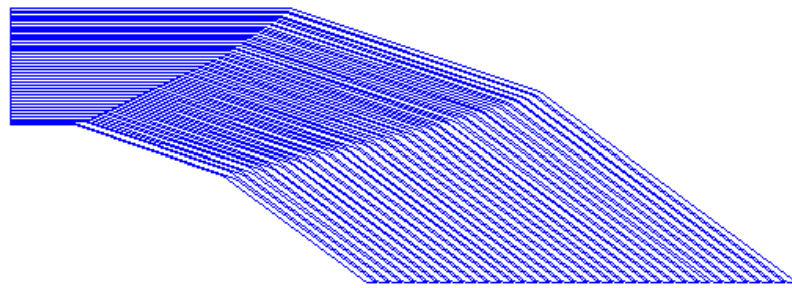
Checking the open trace and show the broken location



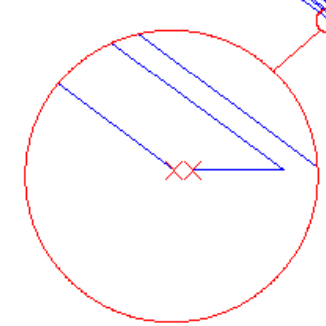
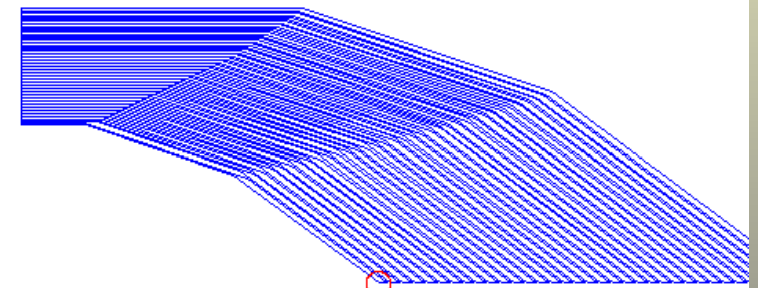
LINE + ARC



PLINE



PLINE

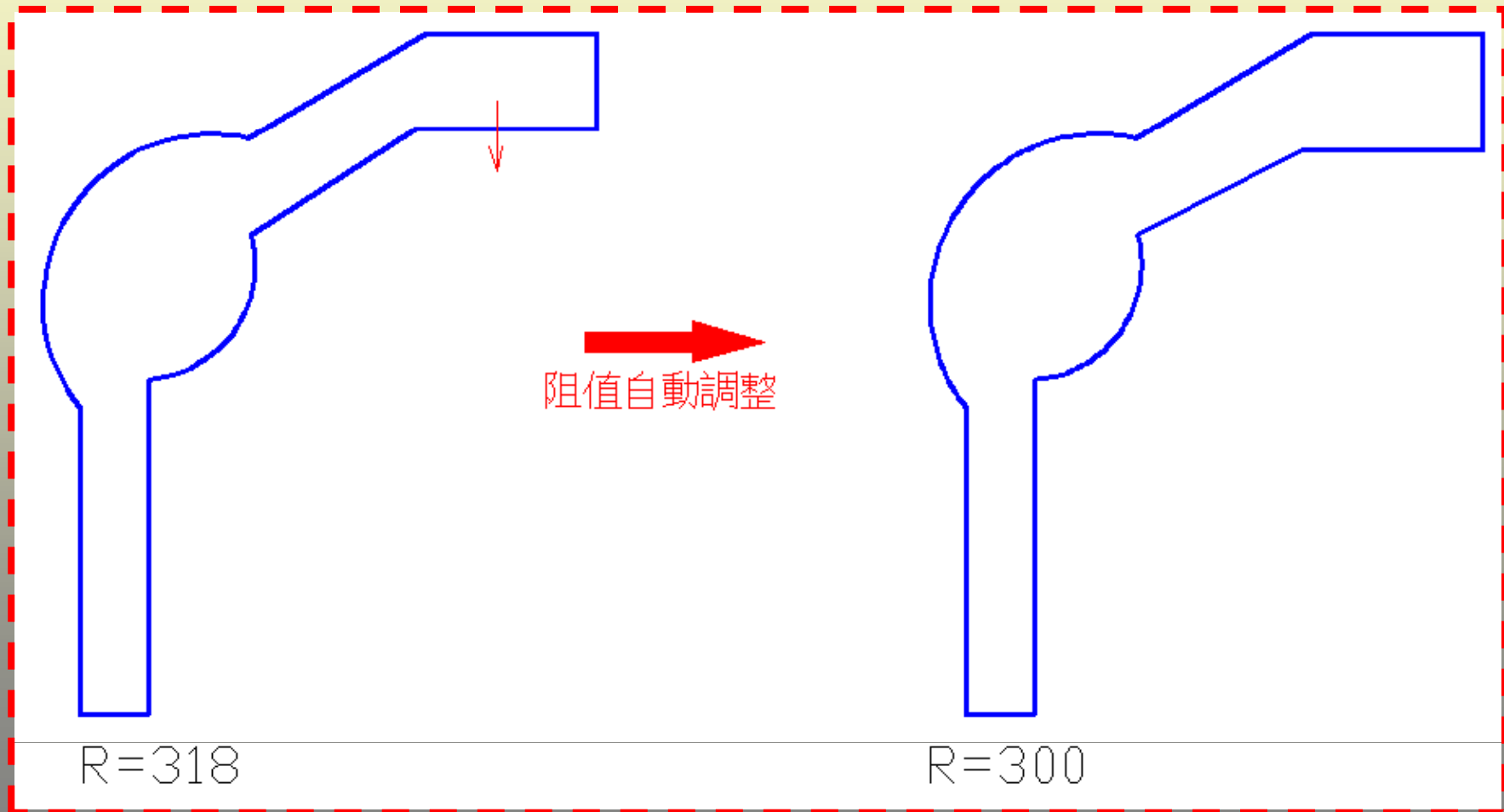


未封閉検査

(6).

Adjust the trace to fit resistance

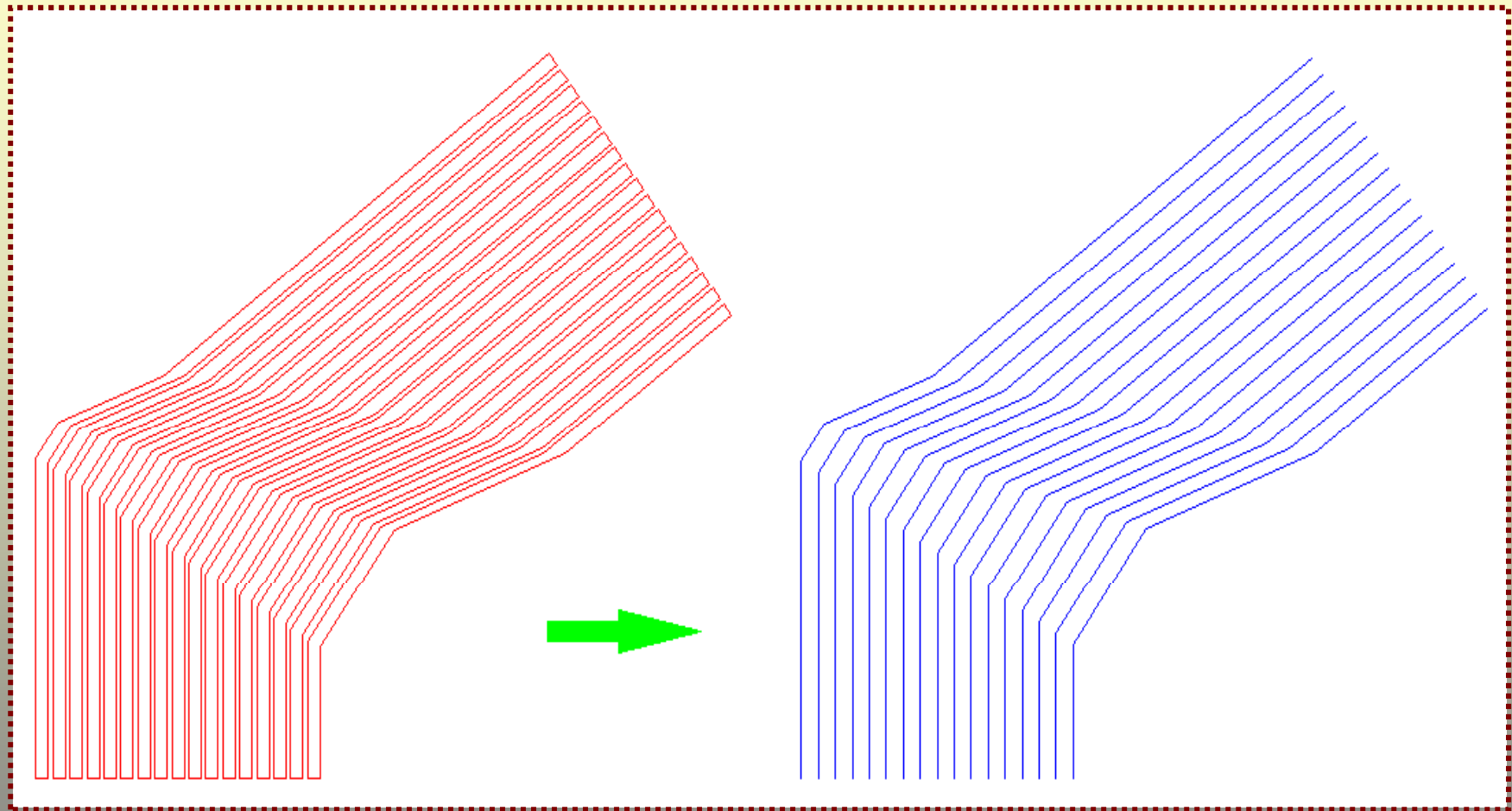
輸入該 **tarce** 期望之阻值,由系統自動調整寬度至最佳化位置



(自動改變邊界線位置以利阻值的調整)

(7).

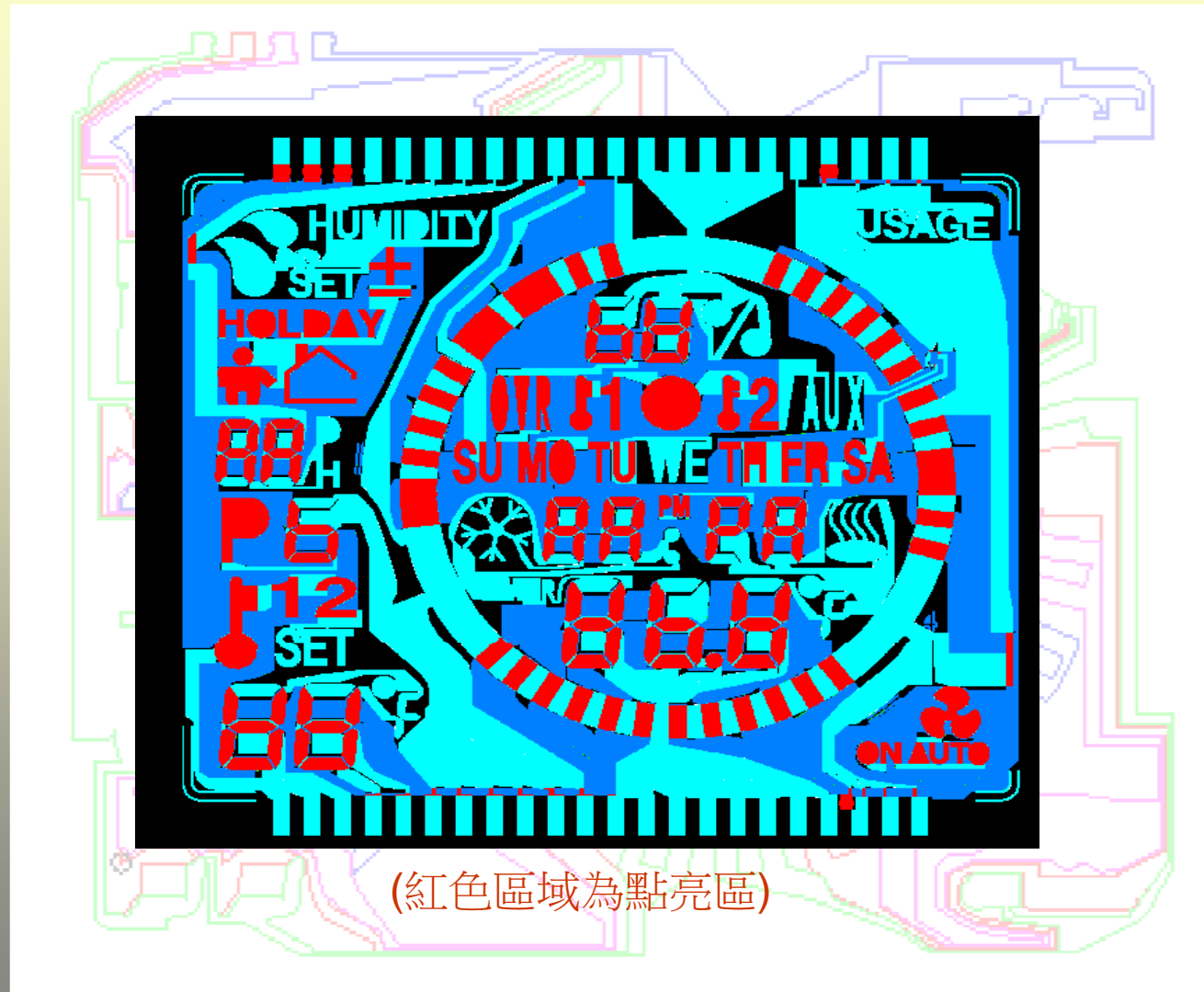
Generate the center line of trace



自動產生 trace (電路)的中心線圖

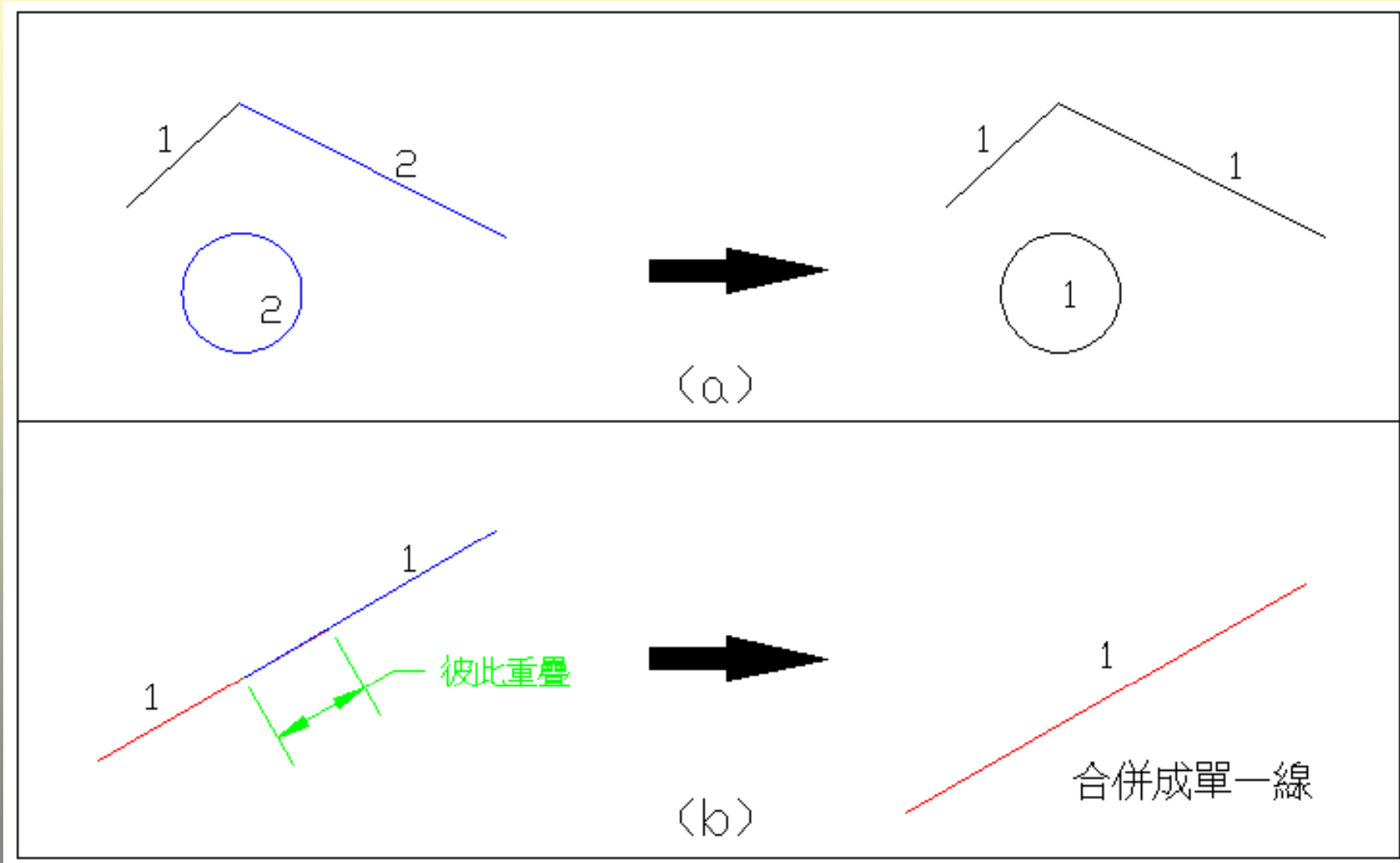
(8).

Preview the result



(9).

Delete layer after object with whole combine to hand over to fold line



Insures the Pline object that the electric circuit can be single closing

(參)

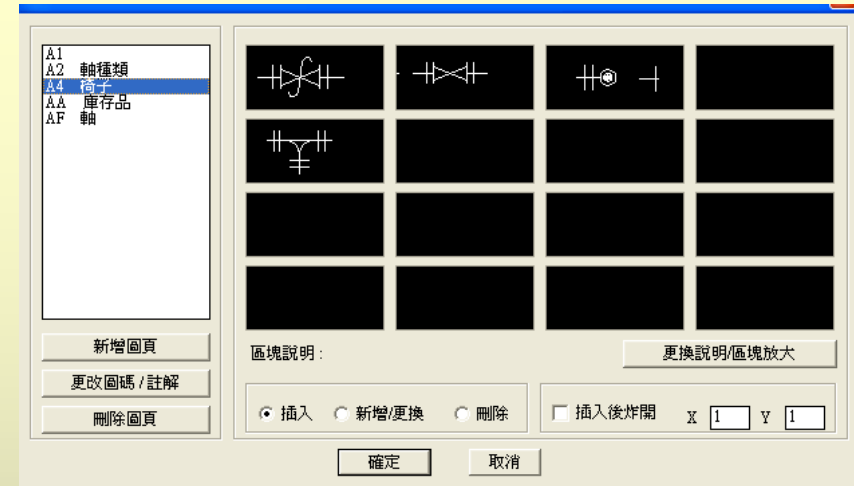
LCD ITO electric circuit support design tools

輔助工具集錦:	▶	圖層ON/OFF作業	▶	
檢測電路特性	▶	重疊物件處理		
BUMP 展繪作業		局部放大處理		
繪製測試電極	▶	統計資訊:	▶	
		線弧串接為Pline		
		導圓/斜角(多選)	▶	
		偏移複製(多選)		
		刪除指定物件	▶	
		文字連續編號	▶	
		文字處理:	▶	文字屬性處理
		繪製陰影BOX		文字大小寫轉換
		不等比例縮放		書寫外部文字檔(txt)
		繪製晶片座		文字繞Pline寫
		線弧百分比位置		模穴編號作業
		物件屬性轉換:	▶	文字相對位置複製
		產生物件的邊界線	▶	繪製表格(FORM)
		打斷(break)物件		



Support design tools :

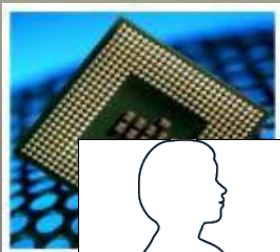
- (1). Read into the exterior text file
- (2). Delete particular object
- (3).統計數量與線長
- (4).不等比例縮放
- (5).Diagram layer On/Off
- (6).文字相對位置複製
- (5). 一次倒斜角
- (6). 物件打斷
- (7). 表格快速繪製
- (8). 電路曲折繪製
- (9). 模穴快速編號
- (10). 面積統計
- (11). 繪製間格線
- (12). 線弧百分比位置
- (13). 中英文詞庫管理
- (14). 圖庫(block)管理
- (15). 刪除長度為零的線段
-etc.



(圖庫管理)

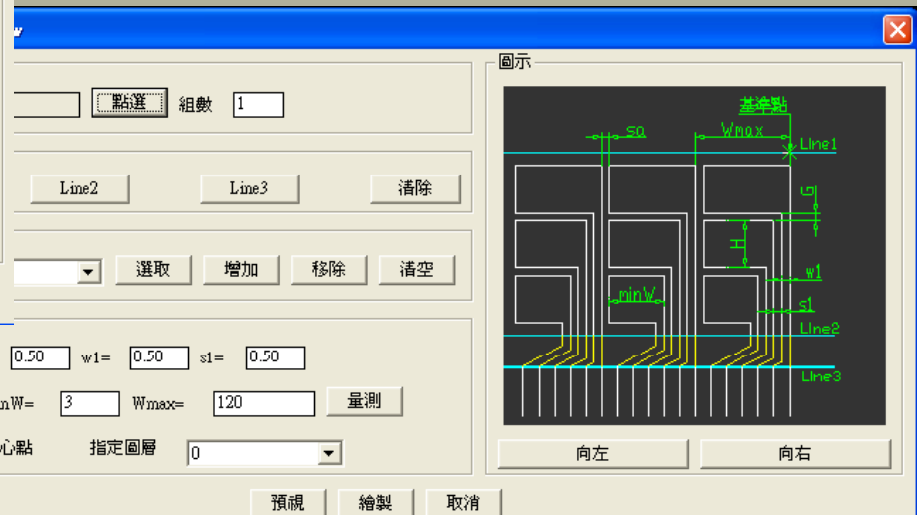
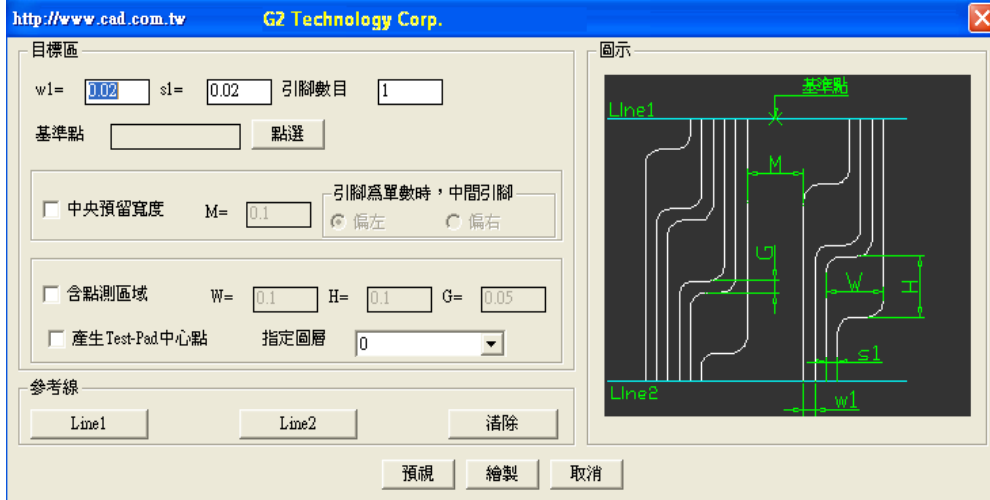
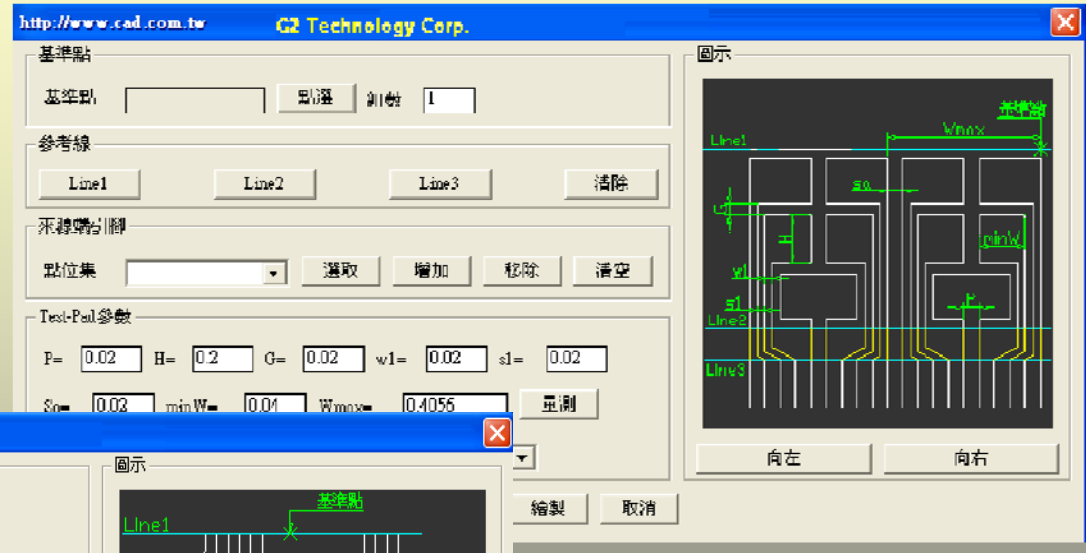


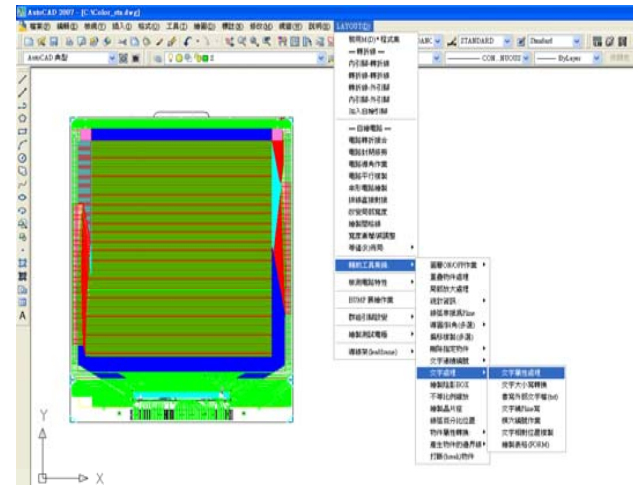
(中英文詞庫管理)



(肆)

FPC / COF testpad drawing





(for AutoCAD based)